SIEMENS

Design Examples of Semiconductor Circuits

Edition 1974

SIEMENS AKTIENGESELLSCHAFT

The circuit designs and descriptions in this booklet are to demonstrate by examples the manifold applications of semiconductors.

To offer a good survey, cases of similar applications have been grouped in chapters.

No guarantee is given for the circuits as far as patent licences are concerned.

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Part I

Preface

The semiconductor circuits described in this booklet cover a broad range of applications. The major part of the circuits were developed and tested in the Siemens Application Laboratories for Semiconductors. Cases of preliminary designs and suggestions are specially indicated in the respective chapters.

As we have again a whole series of new semiconductor components, the respective possiblities of application have been selected and described.

Furthermore, new circuit concepts are presented as, for instance, for the use of optoelectronic couplers, double magneto resistors, triple diffused transistors and epibase darlington transistors, high-sensitivity photo circuits, new RF power supplies with mains separation for AF and TV sets as well as projector lamps.

Among RF applications, we find circuits using the AM- tuning diode BB 113, a FM tuner and a FM receiver set operating with integrated circuits.

The field of TV is covered by descriptions of a thyristor colour H deflection, a medium-voltage transistor deflection and deflection circuits for b/w portable TV sets. Moreover, circuits for a TV sync generator, a white-field and a colourbar generator are presented.

Applications of light-emitting diodes, high-speed diodes, thyristors and triacs as well as AF amplifiers using new epibase darlington transistors are shown.

In cases where graphical symbols have not yet been introduced for the new components, you will find suggestions. When an additional grouping remains unstated in the circuit diagrams for the transistors this means that all groups of the respective type may normally be used. Only in special cases, a more defined limitation could become necessary.

1. AF Circuits

1.1 Headphone amplifiers (NL-7259)

The headphone amplifier shown in Fig. 1.1. corresponds to the Hi-Fi standard with respect to distortion factor and voltage frequency response. Its high input resistance of about 250 kΩ permits universal application. The headphone is connected d.c. current-free.

The amplifier has an A-output stage T_3 operating into a current impressing circuit T_2, D_1, D_2. Larger ranges of dynamic and operating voltage are thus achieved so that headphones may be connected having resistances of 200 to > 2000 Ω.

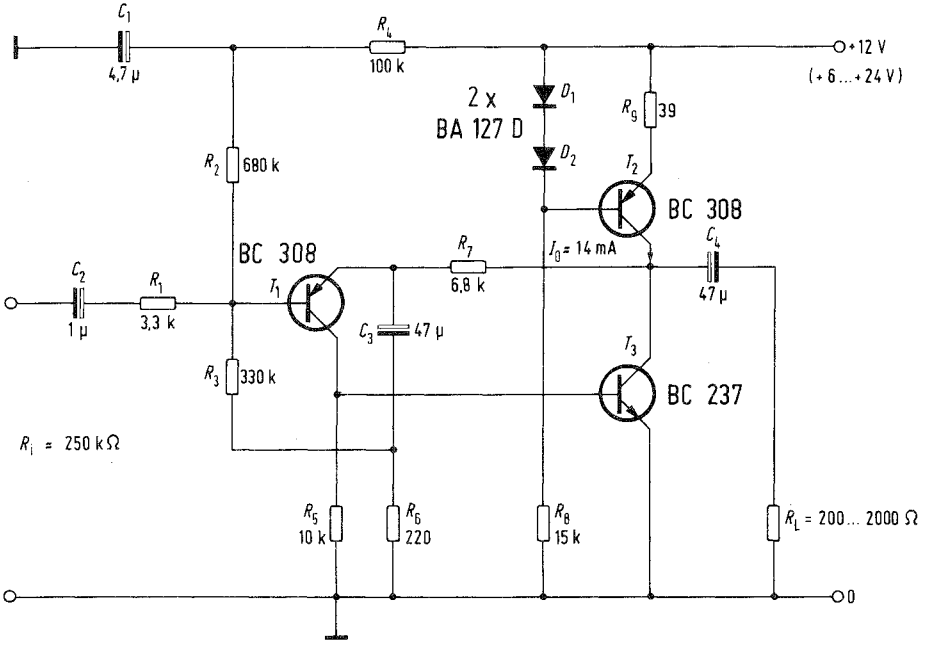


Fig. 1.1

Through the high internal resistance of transistor T_2 a very favourable hum-reduction factor to the output is further obtained.

The output depends on the headphone resistance and the operating voltage.

Technical data:

Operating voltage	12 V (6 to 24 V)
Current consumption	14 mA
Input resistance	250 kΩ
Voltage frequency response (— 1 db)	
at $R_L = 200\ \Omega$	37 Hz to 470 kHz
Voltage gain	25
$V_{o\ nom}$ ($k = 1\ \%$, $f = 1$ kHz) $R_L = 200\ \Omega$	1.5 V (11 mW)
$R_L = 2000\ \Omega$	3.4 V (6 mW)
Distortion factor ($R_L = 200\ \Omega$, $V_o \leqq 1$ V)	0.5 %
($R_L = 2000\ \Omega$, $V_o \leqq 3$ V)	0.1 %

1.2 Hi-Fi mixer amplifier with tone control (NE-7309)

The mixer amplifier shown in Fig. 1.2 consists of a mixer stage having three separate inputs, an active tone control and a summation loudness control being true to hearing.

The input sensitivity was chosen in a manner to permit direct connection of the major part of AF signal sources, such as radio receivers, tape recorders, equalizing amplifiers, etc. Appropriate preamplifiers are to be used if magnetic pick-ups and microphones are connected. An additional dropping resistor of 0.4 MΩ at the input control will suffice if a crystal pick-up should be connected.

The mixer controls at the input of prestages offer the advantage that almost any size of input signal may be processed.

Mixer stages having a voltage gain of 3 will drive the active tone control at low-ohmic values. In the following two-stage amplifier the voltage is amplified by a factor of 5 so that the nominal output voltage is 1.5 V. The majority of power amplifiers may thus be driven.

The summation loudness control has a disconnectable correction of the frequency response which is true to hearing and depends on the loudness. For a simple loudness setting true to hearing, however, a 100 kΩ potentiometer may be used at point A instead having a tap of approx. 1/3 to 1/2 of the full value, or only a logarithmic potentiometer of 50 to 100 kΩ. The load resistance at the output of the loudness control true to hearing should be > 25 kΩ.

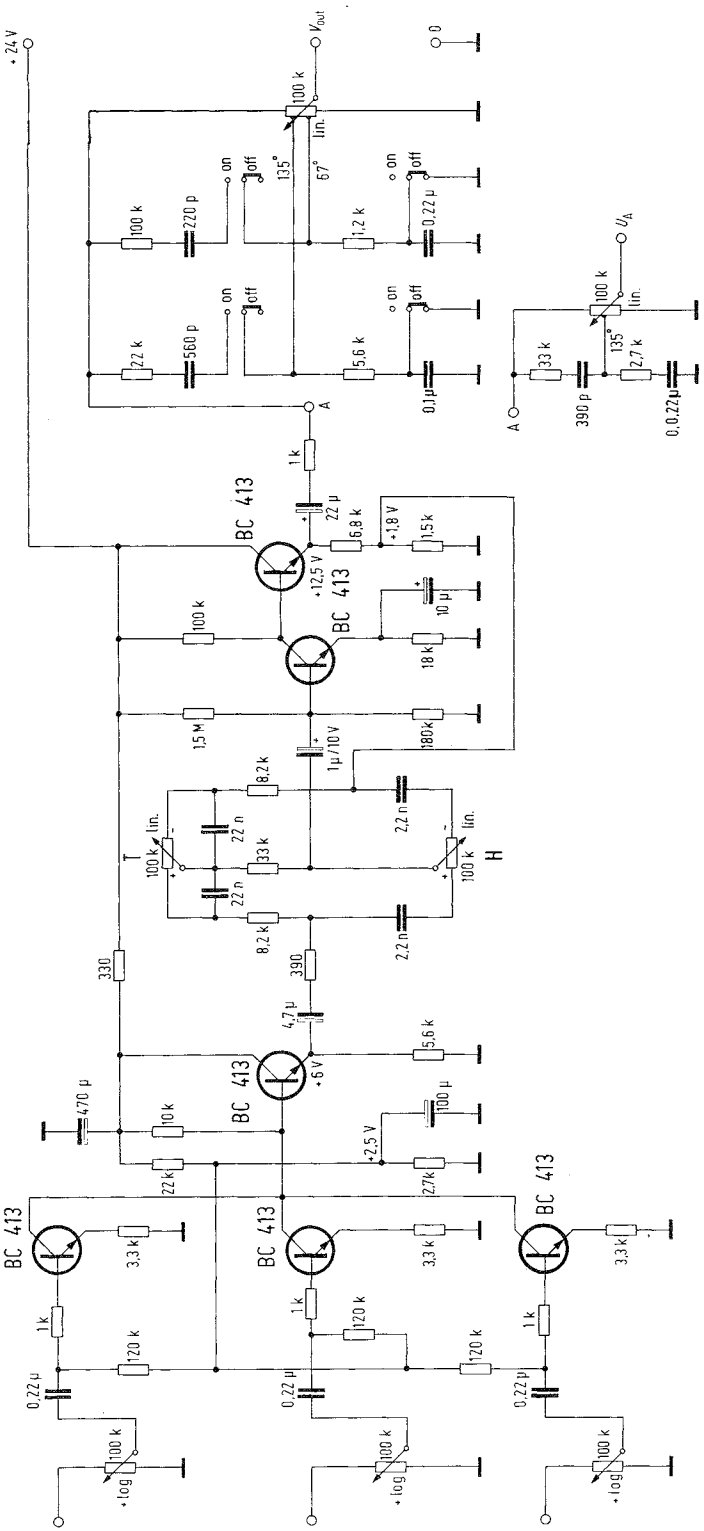

+24 V
V_{out}
0
100 k
lin.
135°
67°
on
off
100 k
220 p
1,2 k
0,22 µ
2,2 k
560 p
5,6 k
0,1µ
A
1 k
22 µ
BC 413
+12,5 V
+1,8 V
6,8 k
1,5 k
10 µ
18 k
100 k
1,5 M
180k
1 µ/10 V
8,2 k
2,2 n
33 k
22 n
T
H
330
390
4,7 µ
+6 V
5,6 k
470 µ
10 k
100 µ
+2,5 V
22k
2,7k
3,3 k
120 k
0,22 µ
log
U_A
33 k
390 p
2,7 k
0,0,22µ

Fig. 1.2

Technical data:

Operating voltage	24 V
Current consumption	5.5 mA
Nominal input voltage	100 mV
Input resistance	50 to 100 kΩ
Voltage gain	15
Nominal output voltage	1.5 V
Max. output voltage (k = 1 %)	5 V
Distortion factor (V_o = 1.5 V, f = 30 Hz to 16 kHz)	< 0.3 %
Voltage frequency response (— 1 db)	13 Hz to 45 kHz
Setting range of tone control:	
bass 50 Hz	+ 17 to — 19 db
treble 16 kHz	+ 18 to — 18 db
Extraneous output voltage DIN 45 405	0.6 to 1 mV

1.3. AF amplifier 10 to 25 W/4 Ω with BD 675/676 (NL-7252)

When the epibase darlington output stage BD 675/676 in the SOT 32 case is directly driven by the integrated circuit TAA 761 A a maximum output power of 25 W is achieved with 4 Ω.

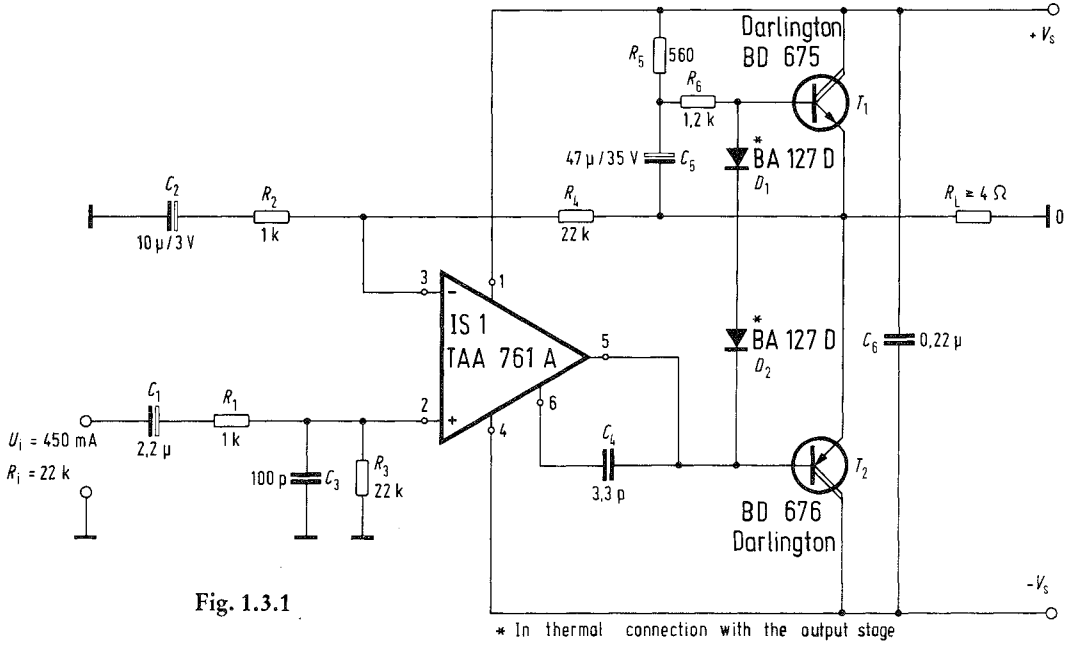


Fig. 1.3.1

The output power is limited mainly by the maximum permissible operating voltage of the TAA 761 A. Amplifiers with an output power of 10, 15, 20 and 25 W and a capacitive and d. c. coupling of the loudspeaker are shown and their technical data are listed in the following table (**Fig. 1.3.1 and 1.3.2**).

These amplifiers offer the following advantages over the version using single semiconductor prestages:

1. no closed-circuit current setting
2. no emitter resistors
3. hence, about 20 % higher output power.

The somewhat higher distortion factor with lower dynamic values proves disadvantageous. In case short-circuit proofing is required points 2 and 3 are omitted. Short-circuit proofing is more difficult to achieve because of the higher amplification and thus stronger tendency towards oscillations.

Technical data of amplifiers with d. c. coupling according to **Fig. 1.3.1.**

Nominal output power					
$P_{o\,nom}$ ($k = 1$ %)	10	15	20	25	W
Load resistance	4	4	4	4	Ω
Operating voltage	+ 10.5	+ 13	+ 14	+ 15.5	V
	— 12	— 14.5	— 15.5	— 17	V
Current consumption $P_o = 0$		≈ 10 mA			
$P_{o\,nom}$	0.72	0.88	1	1.1	A
Nominal input voltage	0.29	0.35	0.4	0.45	V
Input resistance	22	22	22	22	kΩ
Voltage frequency response (— 1 db, $1/2\ P_{o\,nom}$)		23 Hz to 40 kHz			
Output power frequency response (— 1 db, $k = 1$ %)		20 Hz to 30 kHz			
Distortion factor at $1/2\ P_{o\,nom}$, 50 Hz to 15 kHz	0.3	0.3	0.3	0.3	%
0.1 W to $P_{o\,nom}$ 50 Hz to 15 kHz	< 1	< 1	< 1	< 1	%
Thermal resistance of heat sink per output stage transistor	14	9	7	5	K/W

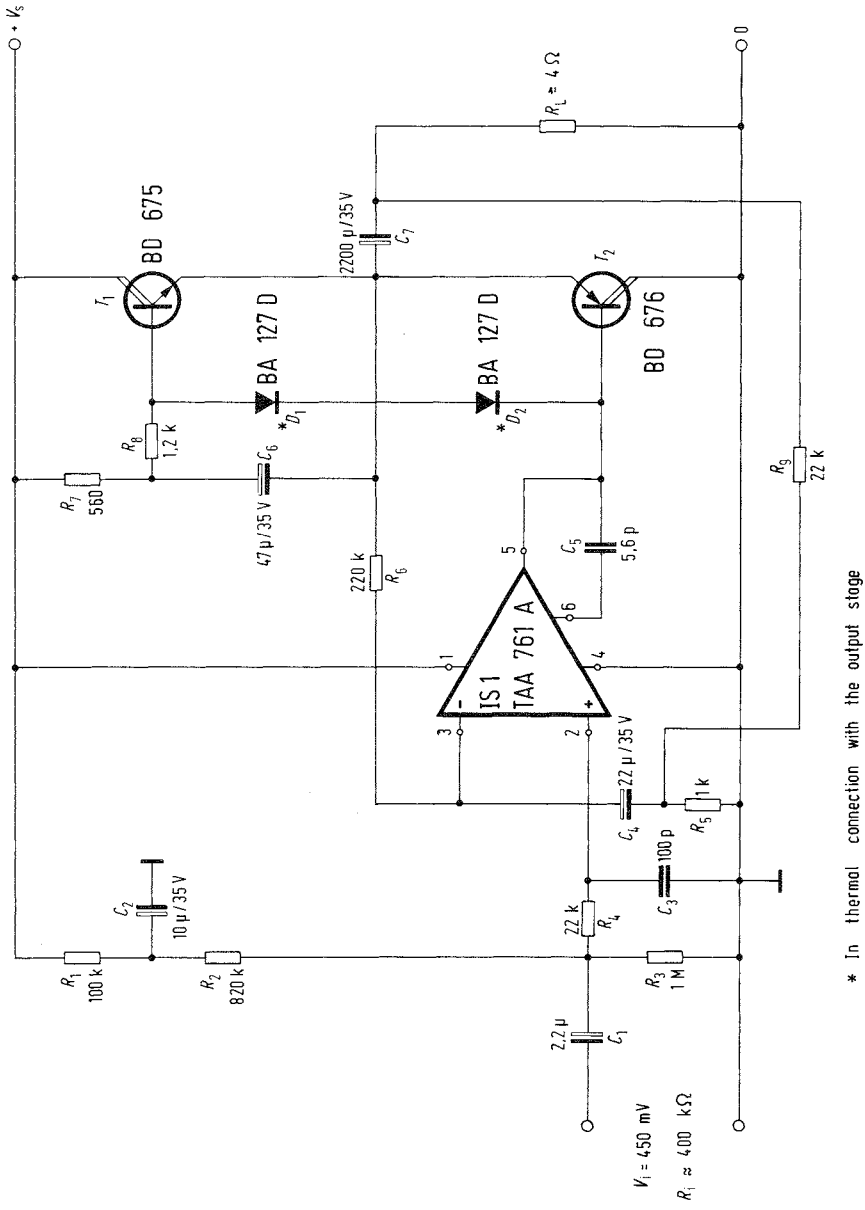

+ V_S
0
$R_L \approx 4\,\Omega$
BD 675
T_1
BD 676
T_2
BA 127 D
$*D_1$
BA 127 D
$*D_2$
2200 µ / 35 V
C_7
R_8 1.2 k
R_7 560
C_6 47 µ / 35 V
220 k R_6
C_5 5.6 p
IS 1 TAA 761 A
R_9 22 k
C_4 22 µ / 35 V
R_5 1 k
C_3 100 p
C_2 10 µ / 35 V
R_4 22 k
R_1 100 k
R_2 820 k
R_3 1 M
C_1 2.2 µ
V_i = 450 mV
$R_i \approx 400$ kΩ
* In thermal connection with the output stage

Fig. 1.3.2

With the amplifier driven to low signals, the distortion factor may further be reduced by a stronger inverse feedbak, i. e. by increasing R_2 in circuit 1.3.1 or R_5 in 1.3.2.

The input zero voltage and the input zero current of TAA 761 A cause a d. c. voltage of max. ± 70 mV at the amplifier output in 1.3.2. A zero adjustment therefore becomes unnecessary.

Technical data of amplifiers according to **Fig. 1.3.2**

Nominal output power $P_{o\,nom}$ (k = 1 %)	10	15	20	25	W
Load resistance	4	4	4	4	Ω
Operating voltage	22.5	27.5	29.5	32.5	V
Current consumption (P_o = 0)		≈ 10 mA			
($P_{o\,nom}$)	0.72	0.88	1	1.1	A
Nominal input voltage	0.32	0.4	0.45	0.5	V
Input resistance		400 kΩ			
Voltage frequency response (— 1 db, ½ $P_{o\,nom}$)		35 Hz to 30 kHz			
Output power frequency response (— 1 db, k = 1 %)		30 Hz to 23 kHz			
Distortion factor at ½ $P_{o\,nom}$, 50 Hz to 15 kHz	0.3	0.3	0.3	0.3	%
0.1 W to $P_{o\,nom}$ 50 Hz to 15 kHz	< 1	< 1	< 1	< 1	%
Thermal resistance of heat sink per output stage transistor	14	9	7	5	K/W

1.4. AF amplifiers (NL-7253)

A number of Hi-Fi AF amplifiers with output powers of 10 to 50 W, with and without short-circuit proofing, were developed with the new epibase complementary pair BD 645/646. The typical output power of this darlington output stage is approximately 30 to 40 W.

The darlington transistors permit particularly economic design concepts for outputs above 10 W as the complementary driver and their heat sinks may be dropped. Moreover, the plastic package TOP-66 is characterized by low space requirements and easy assembling.

Contrary to the quasi-complementary design concepts there is virtually no rise in the distortion factor in case of a small output power due to the symmetrical design of the complementary output stage. The closed-circuit current stability of the darlington stage is sufficient.
Two amplifier design concepts based on discrete semiconductors are being shown.

I. A quartet-circuit with a capacitive loudspeaker coupling
Fig. 1.4.1

II. Circuit with symmetrical current supply, short-circuit proofing and d. c. coupling of speaker
Fig. 1.4.2

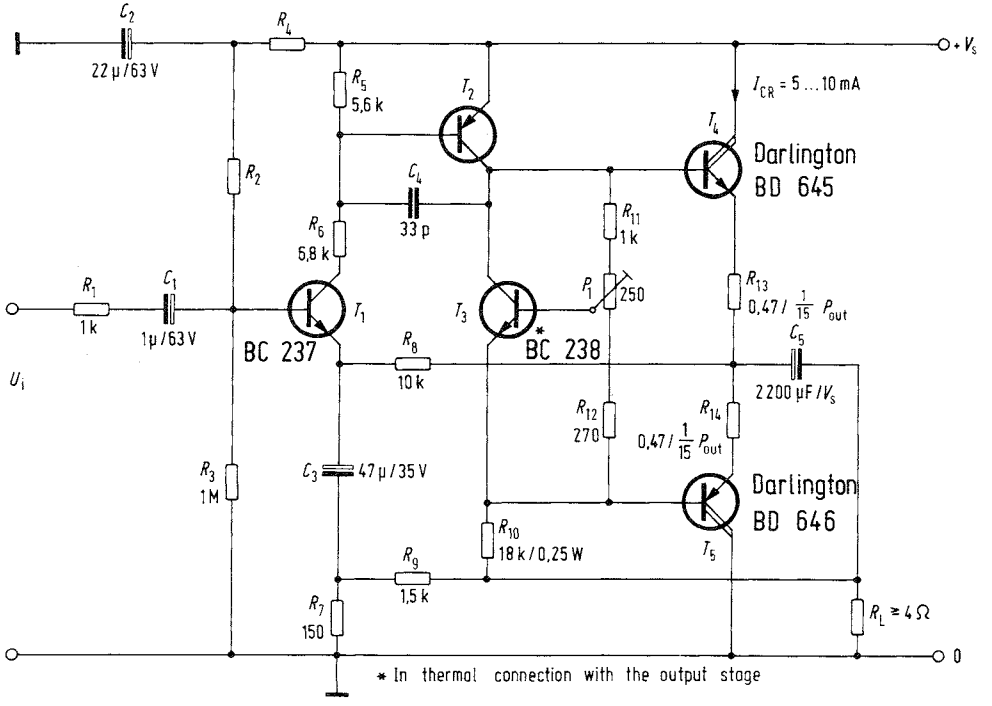
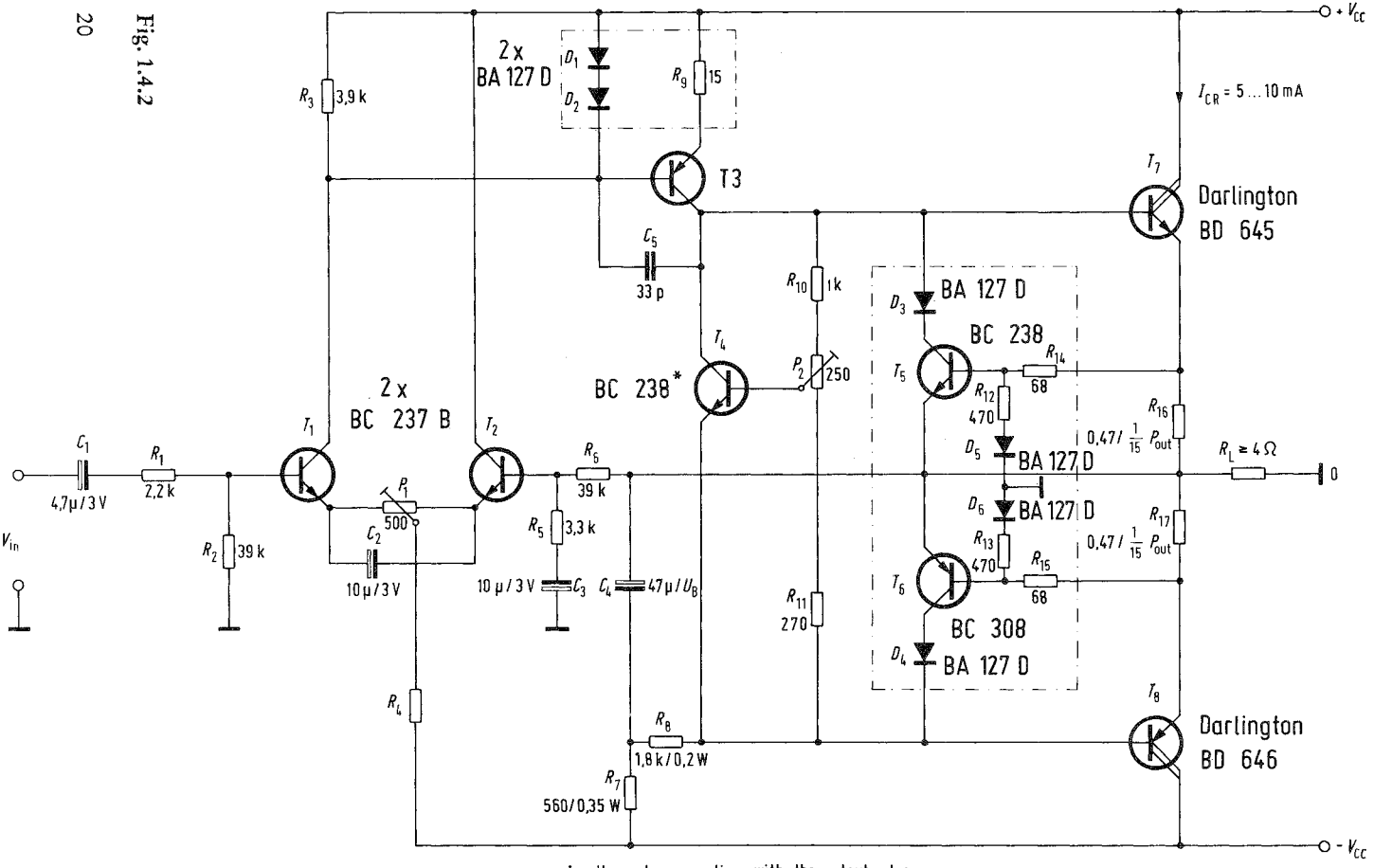


Fig. 1.4.1

Fig. 1.4.2



* In thermal connection with the output stage

Table 1 Technical data of amplifiers

	Circuit Fig. 1.4.1					Circuit Fig. 1.4.2					
Nominal output power ($k = 1$ %)	10	20	30	40	50	10	20	30	40	50	W
Operating voltage	25	33	39	45	49	+13	+17	+20	+23	+25	V
						−12	−16	−19	−22	−24	V
Current consumption $P_o = 0$	13	14	15	16	17	13	14	15	16	17	mA
$P_{o\,nom}$	0.75	1.05	1.25	1.43	1.58	0.75	1.05	1.25	1.43	1.58	A
Load resistance						4 Ω					
Nominal input voltage	0.5	0.7	0.9	1	1.1	0.5	0.7	0.9	1	1.1	V
Input resistance		> 300 kΩ							39 kΩ		
Distortion factor at 0.8 $P_{o\,nom}$					< 0.5 %						
Distortion factor at $P_o = 100$ mW					≦ 0.2 %						
Voltage frequency response (— 1 db)					≈ 20 Hz to > 60 kHz						
Output power frequency response (— 1 db, $k = 1$ %)					≈ 30 Hz to 30 kHz						
Thermal resistance of heat sink per output stage transistor R_{thHS}	≦ 15	8	5.5	4.5	3.5	7	5	4.5	4	3.5	K/W
for driver transistor R_{thHS}	≦ —	—	—	—	—	—	—	90	90	80	K/W

Table 1 shows the technical data of amplifiers and **Table 2** the data of the variable components. Only a few components have to be varied in both circuits in order to achieve various power outputs. The output stage quiescent current should be about 5 to 10 mA. It is set by means of the 250 Ω trimmer. Transistor BC 238 serves to stabilize the temperature of the closed-circuit current and must be in thermal contact with the output stage (mounted to the heat sink). A rise in the closed-circuit current in case of high temperatures will influence neither the transmission properties of the amplifier nor the maximum output power obtainable. Only in case of a small output power the efficiency will slightly be reduced.

Table 2 Data of variable components

$P_{o\ nom}$	10	20	30	40	50 W
	Circuit Fig. 1.4.1				
R_2	620	680	750	750	750 kΩ
R_4	100	100	68	68	82 kΩ
T_2	BC 307	BC 307	BC 327	BC 161	BC 161
	Circuit Fig. 1.4.2				
R_4	22	27	39	39	39 kΩ
T_3	BC 327	BC 327	BC 327	BC 161	BC 161

2. RF Circuits

2.1 AM tuning diode BB 113

The advantages offered by the use of tuning diodes are generally known.

In UHF and VHF tuners tuning diodes have found wide acceptance. In these frequency ranges switching diodes too are frequently used or becoming more and more important. After the development work in these fields has largely been completed, the problems of the AM range have to be solved (HF, MF and LF). Siemens developed the tuning diode BB 113 for the AM range. It has three equal systems on one crystal. These result in equal initial and end capacitance values via the tuning voltage, i. e. in good tracking. The individual partial diodes are balanced in a very favourable manner so that any interference becomes impossible with the normal amplifications of a RF stage (up to 20 db). To this end an adequate internal ground connection has been provided for.

2.2 Large-signal proof RF amplifier or mixer with 60-Ω-input (HL-7212-06)

Fig. 2.2 shows the respective circuit which was designed and tested. The amplifier stage is a high-current stage represented by transistor BF 241, the collector current being set to 5 to 6 mA.

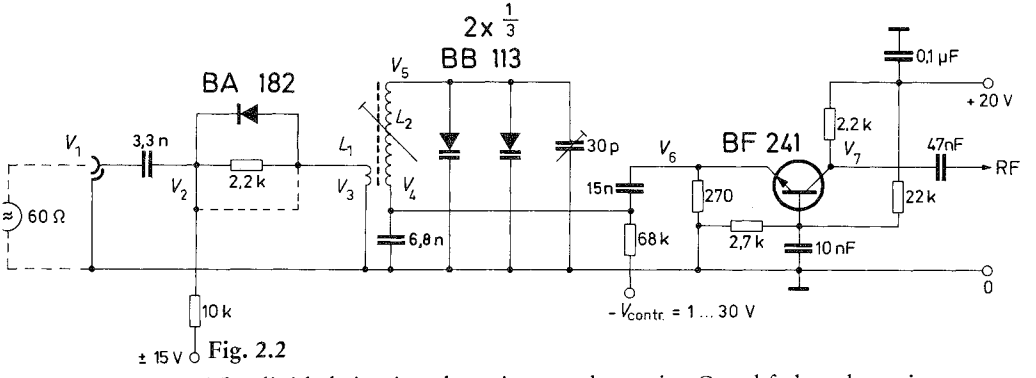


Fig. 2.2

The divided circuit voltage is tapped at point C and fed to the emitter. This coupling offers the advantage that the load transformation changes as a function of frequency. At low frequencies a better circuit attenuation may be achieved than at high frequencies, i. e. the selection may be maintained more uniformly over the frequency range.

The antenna coil is designed for connection to 60 Ω. A "switching mechanism" incorporating the switching diode BA 182 is connected to this coil. When the diode is switched to forward direction the antenna signal may proceed to the antenna coil without any noticeable loss. When the diode BA 182 is reversed the 2.2 kΩ resistor divides the signal to approx. 1/30.

Coil data: Coil D 41 — 2519 (Vogt)
L_1 = 2 turns Cul S 0.1
L_2 = 100 turns, stranded wire 5 × 0.05 Cul/S

This sensitivity change-over has the advantage that the selection remains the same and that the bandwidth does not change to any considerable degree; the detuning too remains in permissible bounds.

Tables 1 and 2 list the measuring results for the RF amplifier. It is to be noted that input signals up to approximately 100 mV_{ss} ($R_{in} \approx$ 60 Ω) may be processed without large modulation distortions. From this point of view, most of the devices probably do not require any control or sensitivity change-over even if this first stage is simultaneously used as a mixer. The signal conditions for a mixer are described under 2.5.

Table 1 Large-signal measurements (2/3) BB 113 in RF amplifier in common base circuit

		diode on		diode off	
f MHz	Δf (kHz) V_i = 10/100 mV_{ss}	B (kHz) V_i = 10 mV_{ss}	$V_{BB\ 113}/V_{ss}$ V_i = 100 mV_{ss}	B (kHz) V_i = 1 V_{ss}	$V_{BB\ 113}/V_{ss}$ V_i = 5 V_{ss}
0.6	— 1	10	1.5	9	1.5
1	— 0.6	13	3.5	9	2.5
1.5	— 5	25	3.5	13	2.5 (V_i = 2.5 V_{ss})

Table 2 Level conditions of RF amplifier according to Fig. 2.2, page 23, at V_i = 50 mV, R_i = 60 Ω

f MHz	R_{in} Ω	V_1 mV_{ss}	V_3 mV_{ss}	V_4 mV_{ss}	V_5 V_{ss}	V_6 mV_{ss}	V_7 V_{ss}	V_7/V_1	v_p dB	B kHz	$V_{1\ max}$ mV_{ss}
0.6	120	50	15	15	0.67	4.0	1.35	27	16.0	8.1	220
1.0	57	50	40	18	2.15	7.5	2.4	48	17.8	14.5	220
1.5	68	50	50	15	2.85	6.5	2.15	43	17.6	27.0	270

2.3 Input for car superhets with BB 113 (HL-7212-06)

In mobile sets large variations of input signals may be expected on the one hand, and a coarse mismatch of the antenna to the receiver input on the other hand. As to the former, the circuit may be recommended as shown in 2.2.

A car antenna is matched in the most favourable manner only if the tuner is mounted directly (i. e. without a transmission line) at the base of the antenna and only the IF (or AF) is connected to the control panel in the car by means of a usual cable. The diodes are tuned with d. c. voltage fed via shielded cables.

Another possibility is a broad-band, high-resistive matching transformation with a very stable primary/secondary coupling between antenna and superhet input. Unless too large bandwidths are to be covered a circuit may be realized in accordance with Fig. 2.3.1. Here again a 60 Ω or 150 Ω cable may be used.

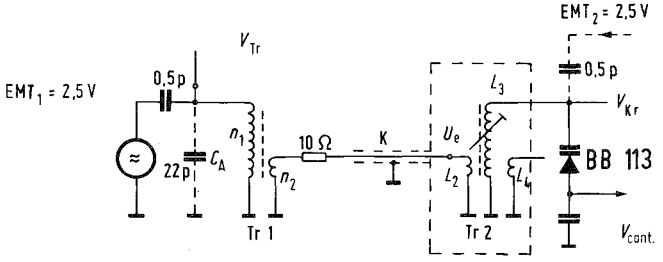


Fig. 2.3.1

Coil data:

Tr 1: Siferrit pot core, ordering code B66541-K 0040-A 033

n_1: 230 turns 12 × 0.05 mm CulS

n_2: 15 turns 0.2 mm CulS

measured by means of a dummy antenna capacitance

C_A = 22 pf instead of a rod antenna A (≈ 22 pf)

K: coaxial input cable 1.5 m, 60 Ω

Tr 2: refer to 2.5, L_2, L_3, L_4

A Siferrit pot core of 14 mm diameter is used as antenna transformer ensuring good coupling of antenna and output winding. To avoid any harmful band-pass filter effect between the primary circuit of the antenna transformer Tr_1 and the tuning circuit Tr_2 a 10 Ω series

resistor is incorporated in the 60-Ω cable line. The resultant low losses have to be accepted. As may be derived from the curves shown in 2.3.2 the transmission ratios are quite good considering that the resonant resistance of Tr_2 is about 2 to 5 times the effective resistance of the transformer Tr_1.

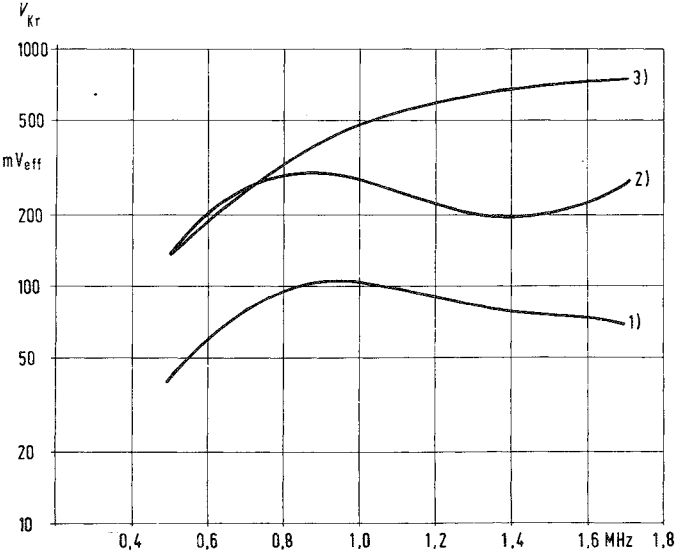


Fig. 2.3.2

Curve 1: Voltage at circuit high-point when fed via antenna transformer (emf_1)

Curve 2: Voltage at circuit high-point when feeding emf_2 with the antenna transformer connected.

Curve 3: Voltage at circuit high-point when feeding emf_2 with the antenna transformer disconnected.

2.4 Oscillator with BB 113 (HL-7212-06)

Among other things an oscillator has to supply as constant a signal for the mixer stage as possible. For example, approximately 100 mV_{ss} with a small generator resistance (100 to 200 Ω) are desired. At $V_R = 1$ V, the circuit voltage across diode BB 113 shall be $V_2 < 1.3\ V_{ss}$ and at $V_R = 30$ V it shall be 2.5 V_{ss} in order that the tracking will remain uninfluenced. Due to the resonant resistance which highly varies with frequency a constant amplitude of oscillations cannot be achieved without taking special measures.

The tuning diode, however, may have varying signals depending upon the tuning voltage.
Supply voltage stabilization is recommended in order to increase the stability of frequency and amplitude.
Fig. 2.4 shows an oscillator circuit for the MF range. It is basically suitable for 10 MHz and above if the overall collector resistance is reduced accordingly (5 kΩ). The transistor is operated in common emitter circuit. The load on the feedback winding is thus to be kept low. The unbridged part of the emitter resistance, as a result of its inverse feedback effect, leads to an increase of the base input resistance. However, the base input voltage required thus rises. Therefore, and as the oscillator circuit is decoupled by the 39 kΩ resistance of the collector resistor the oscillator circuit may emit sinusoidal oscillations while the collector is driven hardly and supplies highly rounded to almost rectangular oscillations which, however, are highly constant with respect to their amplitude.

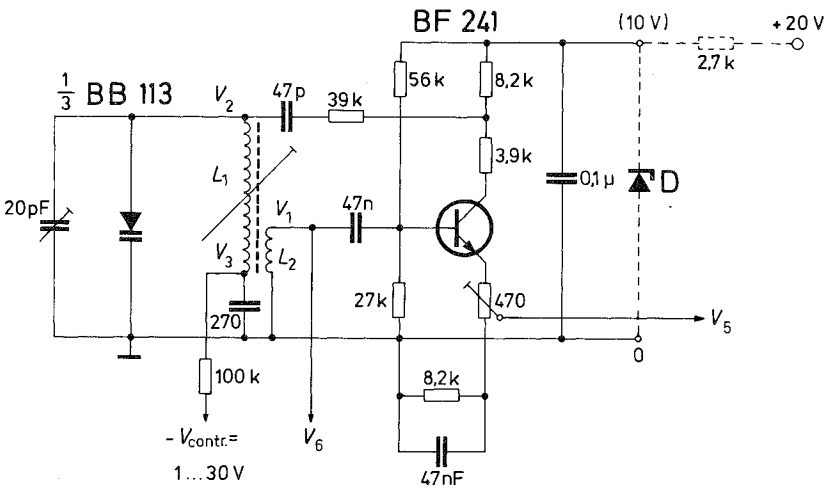


Fig. 2.4

Coil data
L_1 = 100 turns 5 × 0.05 CulS
L_2 = 20 turns 0.1 CulS
Tapping after 5 turns
Coil 041—2640 (Vogt)

The oscillator signal may now be taken from the tapping of L_2 with a sufficient amplitude stability, provided it has a very good sinusoidal shape*, and fed to the mixer. A less sinusoidal voltage V_5, showing however a good amplitude stability, may be taken from the 470 Ω setting resistor when the tap is set to approximately 150 Ω. Further switching contacts may thus be avoided in case of different wave bands.

The following **table 3** comprises the measuring values for the oscillator according to **Fig. 2.4.** It may be derived that the tuning diode is operated in a manner that its limit drive is well utilized. With the oscillator put in front sufficient energy will become available for the mixer stage so that any further buffer stage will become superfluous.

The temperature dependence of the oscillator frequency is caused by the coil. The frequency drift is best compensated for by the tuning voltage by giving it a certain temperature response.

Table 3 Oscillator measuring values according to **Fig. 2.4**

V_R	1	5	10	20	30	Unit	Remark
V_1	480	550	580	600	580	mV	sinusoidal
V_2	1.2	1.8	2.3	2.5	2.5	V_{ss}	sinusoidal
V_3	1	0.85	0.6	0.3	0.18	V_{ss}	sinusoidal
V_4	340	370	370	360	340	mV_{ss}	k_2-distortion
V_5	92	100	100	97	92	mV_{ss}	k_2-distortion
V_6	94	113	113	118	115	mV_{ss}	sinusoidal

2.5 MF tuner with BB 113 (HL-7212-06)

The circuit shown in Fig. 2.5.1 is a tuner developed for the MF range. The RF amplifier simultaneously serves as mixer. The oscillator part basically corresponds to the oscillator described under 2.4. The IF transformer is to represent a primary load resistance of about 6 to 10kΩ. The secondary load is 330 to 400 Ω.

*) The oscillator voltage does not have to show a sinusoidal shape because in normal (single-ended) mixer operation which is given at $V_{osc} = 100 \rightarrow 200\ mV_{eff}$, considerably stronger oscillator signal distortions occur in the mixer stage itself (half-wave operation).

The oscillator signal is fed into the mixer base at very low-ohmic values so that the RF application to the emitter hardly undergoes any considerable input resistance change over the inverse feedback effect of the remaining base resistance (part of the 250 Ω trimming potentiometer). The trimming potentiometer was only used to study the conditions and may be replaced by fixed resistors. This type of oscillator-mixer coupling largely reduces the influence of large input signals on the oscillator.

The input choke improves matching over the frequency range. The 60 Ω input seems to be the best solution for feeding into the antenna besides the wavemagnet solution. It avoids parallel capacitances which are harmful to the tuning diode and yields good transformation conditions. When connected to high-ohmic antennas (e. g. car rod antennas) the solution according to 2.3 is considered advantageous.

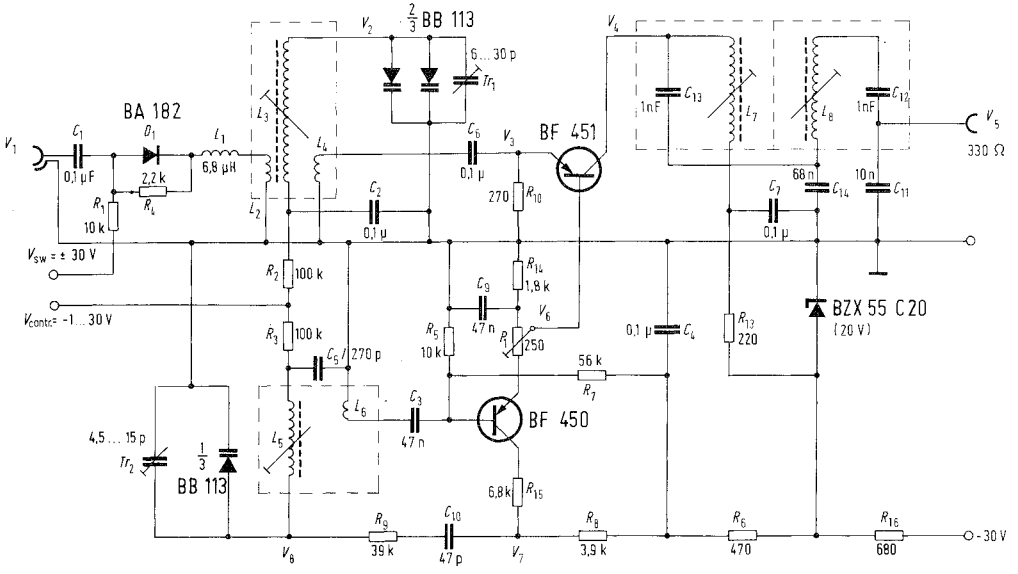


Fig. 2.5.1

The AM tuner shown in **Fig. 2.5.1** has been specially designed to operate only to a reasonable gain (Gp approx. 10 to 15 db). Higher gains will strongly impair the large-signal behaviour. (High gain is

equivalent to a low dynamic range, i. e. a low large-signal compatibility). With a gain of approx. 10 db a sufficiently large signal-to-noise ratio is being obtained.
The diode BA 182 which is provided for at the input serves as a protection against excessive antenna signals, e. g. in case of mobile receiver sets. If this diode is reversed desired signals up to 5 V_{ss} ($R_i \approx 60\ \Omega$!) may be processed. This would correspond to a circuit high-point voltage v_2 of approx. 250 V_{ss}.

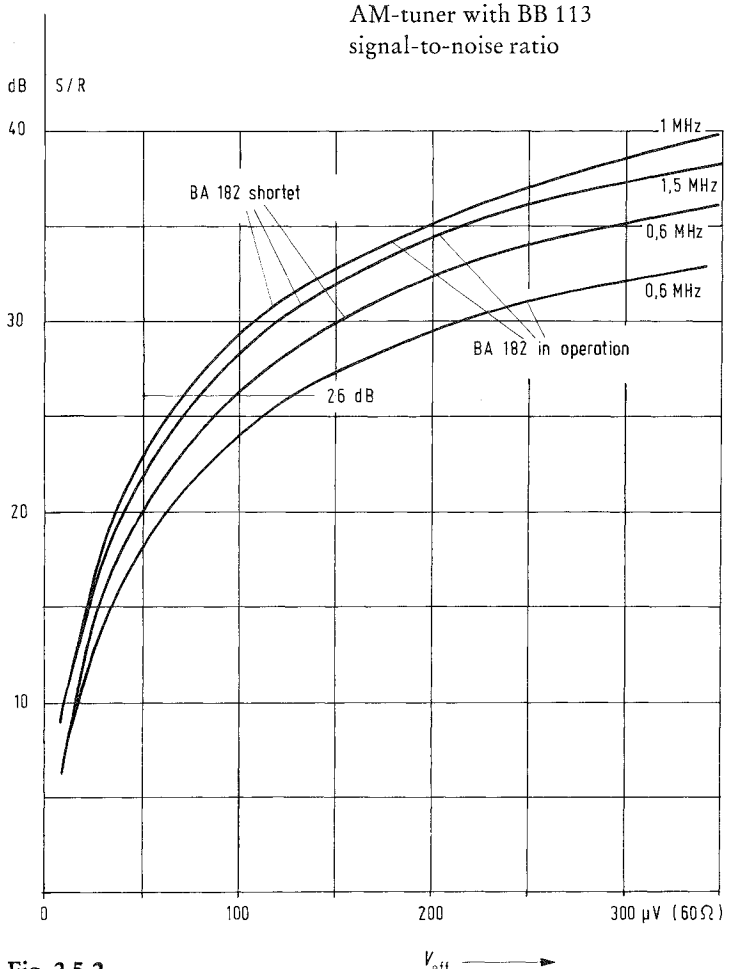


Fig. 2.5.2

The signal-to-noise ratio of the BB 113 AM-tuner with input may be derived from Fig. 2.5.2. The values achieved correspond to those obtainable with mixer input. Better values may be realized with a pure RF prestage, however in this case the equally important large-signal behaviour of such a tuner is bound to deteriorate with the reciprocal value of the added RF amplifier.

Technical data:

Frequency range: 530 to 1620 kHz, IF 465 kHz
Gain: approx. 15 db
Dynamic range at 60-Ω-input ($k_{AF} \leqq 10\ \%$)

	D_1 conductive	D_1 reversed
$V_{in\ max}$ at 600 kHz	85 mV_{ss}	6.5 V_{ss}
$V_{in\ max}$ at 1 MHz	140 mV_{ss}	4.8 V_{ss}
$V_{in\ max}$ at 1.5 kHz	140 mV_{ss}	5.4 V_{ss}

Frequency rejection at 1 MHz: 43 db (D_1 conductive)
IF suppression at 1 MHz: 38 db (D_1 conductive)
Oscillator radio interference at input: 0.9 mV/60 Ω (D_1 conductive)
Oscillator drift at $V_{in\ max}$ and f_{in} 1.5 MHz: $f_{osc} < 0.2$ kHz
$V_{in\ max} = V_1$ in Fig. 2.5

f_{in} MHz	R^*_{in} Ω	V_1 mV_{ss}	V_2 mV_{ss}	V_3 mV_{ss}	V_4 mV_{ss}	V_5 mV_{ss}	V_6 mV_{ss}	V_8 mV_{ss}	G_p db
0.6	35	50	790	11.2	10 400	730	300	1500	13.6
1.0	53	50	710	10.3	10 000	750	340	2400	15.6
1.5	88	50	1040	8.1	8 800	660	340	2800	16.7

*) BA 182 bridged

Coil data:

L_1 = antenna series inductance 6.8 µH 32 turns CuL ⌀ 0.2 mm on core Si 31 s ⌀ 3.3 mm, B 69310-A 0001-X 131
L_2 = antenna coupling to circuit: 2 turns CuLS ⌀ 0.2 mm

L_3 = input circuit 100 turns 4 × 0.05 stranded wire
L_4 = RF coupling winding 1 turn CuLS ⌀ 0.2 mm
L_5 = oscillator circuit 100 turns 4 × 0.05 stranded wire
L_6 = oscillator feedback winding 20 turns 4 × 0.05 stranded wire
L_7 = 1st IF bandpass filter circuit 85 turns stranded wire 12 × 0.04
L_8 = 2nd IF bandpass filter circuit 85 turns stranded wire 12 × 0.04
L_2 to L_8 Vogt filter kit D 41 — 2519

2.6 Stabilization of tuning voltage for BB 113 (HL-7212-06)

The question of the necessary tuning voltage stability is of particular importance. The permissible frequency change of a resonant circuit depends on various factors:

1) the permissible distortion increase of modulation
2) the permissible sensitivity change at circuit
3) the operating frequency (LF, MF or SF).

The SF range marks the highest and the LF range the lowest requirements for stability of the tuning voltage. Assuming a permissible frequency change of $f = 1$ kHz (in absolute terms) as reliable the following approximate values obtained for the LF, MF and SF ranges:

$$\frac{\Delta V_R}{V_R} \text{ for } f = 1 \text{ kHz}$$

for long-wave : 8 ‰
for medium-wave : 3 ‰
for short-wave : 0.3 ‰

The requirements for short-wave are thus 10 times as stringent as for the MF range.

Fig. 2.6.1 and **Fig. 2.6.2** show two stabilization circuits.

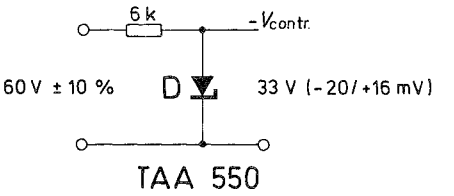


Fig. 2.6.1

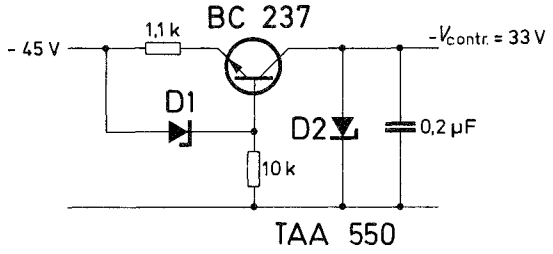


Fig. 2.6.2

2.7. FM-tuner for Hi-Fi sets (HI-7302-01)

A special large-signal proof FM-tuner was developed for use in qualified Hi-Fi sets, as shown in **Fig. 2.7.**

The antenna signal is fed to the tuned RF circuit via a control network with the PIN diodes BA 379, designed as a π section. The transformation from the antenna via the RF circuit to gate 1 of the prestage transistor, a dual-gate MOSFET TV 106, is designed for optimum noise values with as narrow a bandwidth of the RF circuit as possible. The MOSFET output is coupled to a primary circuit tapping of the bandpass filter in order to improve the selection prior to the mixer stage on the one hand, and to keep the prestage gain only at such a level that the noise figure of the mixer constitutes a minor element only in the overall noise figure.

The mixer stage contains the integrated circuit SO 42 P, a symmetrical active ring mixer. The RF input is balanced via a line wound around a ring core. The current-impressing transistors in the SO 42 P are switched as a push-pull oscillator. The IF output is also balanced via a bifilar winding of the coil.

The IF signal is rectified by diode AA 113 and fed to the AGC amplifier which incorporates the operational amplifier TBA 221. Gain and threshold are adjustable, whereas the minimum control level should be set at an antenna signal of 2 mV. The output current of the op amp controls PIN-diodes-attenuator.

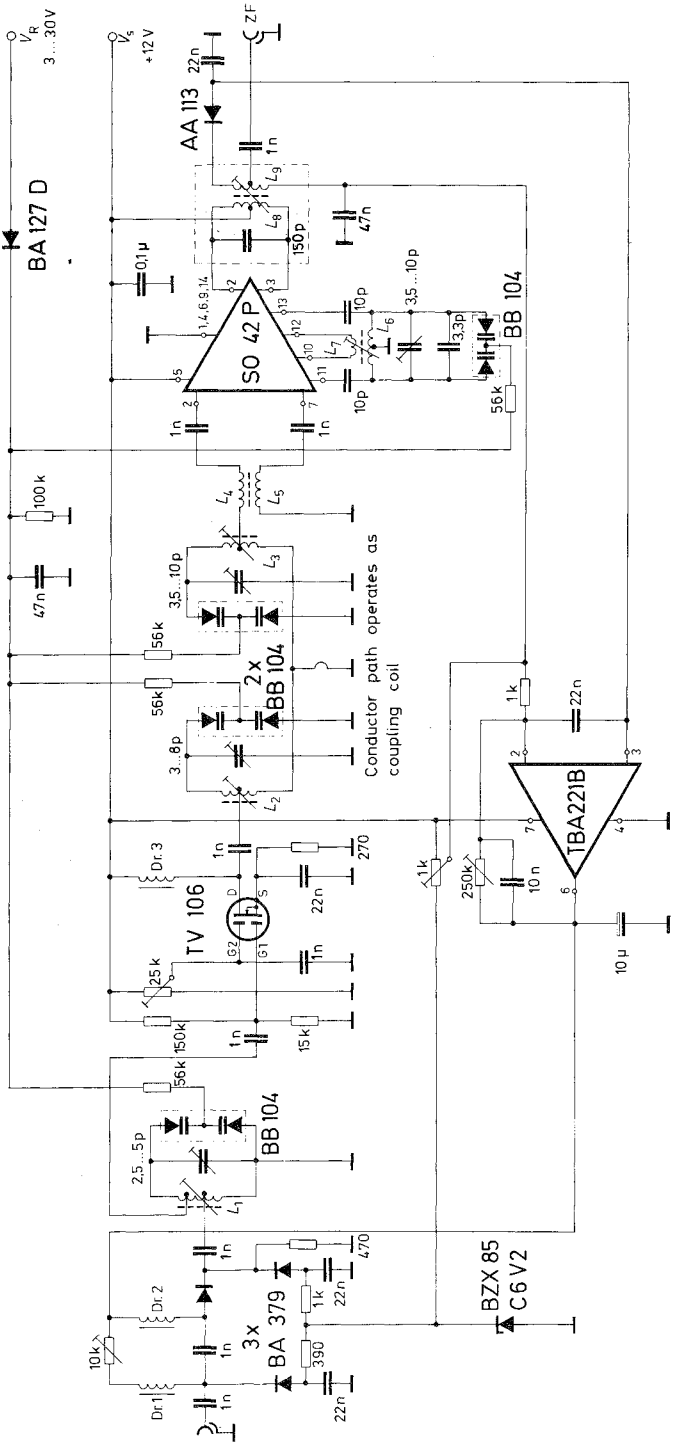

V_R 3...30 V
V_s +12 V
ZF
BA 127 D
AA 113
22n
1n
L_9
L_8
150p
47n
0,1µ
SO 42 P
1.4.6.9.14
2
3
5
7
10
11
12
13
10p
35...10p
L_6
L_7
3,3p
BB 104
56k
1n
L_4
L_5
100k
47n
L_3
35...10p
56k
56k
2x BB 104
3...8p
L_2
Conductor path operates as coupling coil
1k
22n
TBA221B
1k
250k
10n
10µ
270
Dr.3
TV 106
D
S
G2
G1
25k
150k
15k
56k
2,5...5p
L_1
BB 104
470
Dr.2
10k
3x BA 379
1k
390
BZX 85 C6 V2
Dr.1
Input 60 Ω

Fig. 2.7

Technical data:

Operating voltage	12 V
Current consumption	32 mA
Tuning voltage	4.2 to 28 V
Input impedance	60 Ω
Output impedance	60 Ω
Power gain	26 to 28 db
AGC range	> 50 db
Noise figure	4.3 to 4.6 db
RF bandwidth	1.4 to 1.7 MHz

Coil data:

L_1	5.5 turns	0.8 mm ⌀ Cu Ag, tapping after 1/2 turn and after 3 1/3 turns
L_2	5.5 turns	0.8 mm ⌀ Cu Ag, tapping after 3 1/2 turns
L_3	5.5 turns	0.8 mm ⌀ Cu Ag, tapping after 1 1/4 turns
L_6	6.5 turns	0.8 mm ⌀ Cu Ag, center-tap
L_7	2.0 turns	0.5 mm ⌀ Cu L on L_6
$L_{1, 2, 3, 6, 7}$	on coil body Sp 3.5/14.6-2048 (Vogt)	
$L_{1, 2, 3}$	thread core 3.5 × 0.5 × 10.3 made of U 17	
	ordering no. B 63 310-B 3021-X 017	
$L_{6, 7}$	thread core 3.5 × 0.5 × 10, brass	
$L_{4, 5}$	4.0 turns ea., 0.5 mm ⌀ Cu L, twisted on ring core, B 64 290-A 0037-X 001	
L_8	6.0 turns ea., 0.2 mm ⌀, Cu L bifilar	
L_9	6.0 turns,	0.2 mm ⌀, Cu L tapping after 2.0 turns
$L_{8, 9}$	on Vogt filter element D 41-2520	
$Dr_{1, 2, 3}$	10 µH	

2.8 Small FM-receiver set (HI-7302-03)

A small FM set has been developed showing a remarkable input sensitivity despite its simplicity and the small dimensions involved (board 67.5 × 52.5 mm), see **Fig. 2.8.**

The antenna is coupled to the prestage transistor BF 324 either symmetrically with 240 Ω or asymmetrically with 60 Ω with a transducer, the secondary circuit of which constituting a series circuit. A ferrite bead preventing UHF oscillations is interposed between the prestage transistor and the RF circuit tuned with diode BB 104.

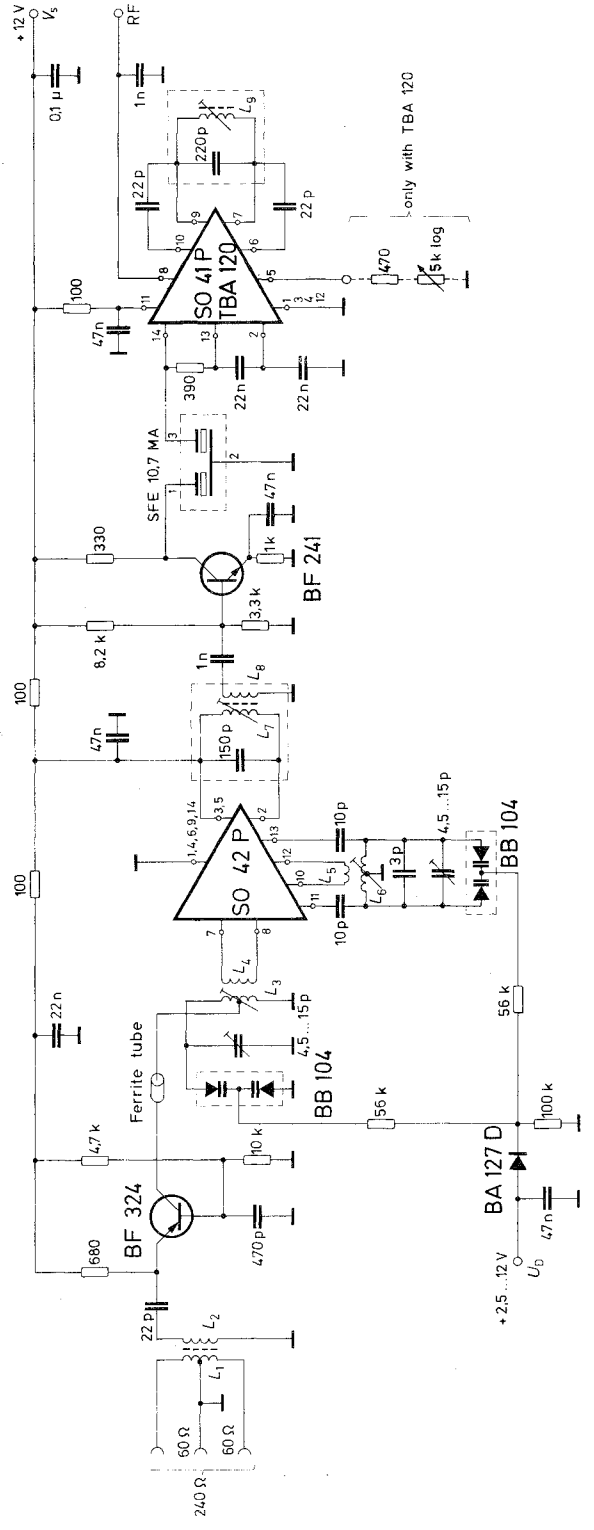

+12 V
V_s
0,1 µ
RF
1n
L_9
220p
22 p
22 p
only with TBA 120
SO 41 P
TBA 120
470
5k log
100
47n
390
22n
22 n
SFE 10,7 MA
47n
330
1k
BF 241
3,3k
8,2 k
1n
L_8
L_7
150 p
47n
100
100
SO 42 P
10p
3p
4,5...15 p
BB 104
10p
L_5
L_6
L_4
L_3
22n
15p
4,5...15 p
BB 104
Ferrite tube
56 k
56 k
100 k
4,7 k
10 k
BF 324
470p
BA 127 D
680
47n
+2,5...12 V
U_D
22p
L_2
L_1
60 Ω
60 Ω
240 Ω

Fig. 2.8

The mixer incorporates the integrated circuit SO 42 P which also actf as an oscillator. The intermediate frequency is coupled out asymmetrically through a parallel circuit and fed to the first IF stage by means of transistor BF 241. The following ceramic filter SFE 10.7 MA is matched at input and output by ohmic resistors in order to obtain optimum characteristics. The spurious response of the filter is sufficiently suppressed by the IF circuit at the mixer output. The limitation and demodulation may selectively comprise the integrated circuit SO 41 P or TBA 120. SO 41 P results in a higher sensitivity with a lower current consumption, however also in a lower AF output voltage than the TBA 120. Moreover, the TBA 120 lends itself to loudness control via pin 5.

Technical data:

	with TBA 120	with S 041 P
Operating voltage	12 V	12 V
Current consumption	27.5 mA	15 mA
Tuning voltage	2.7 to 12 V	
Noise figure	4 to 5 db	
RF bandwidth	1.4 to 2 MHz	
IF bandwidth	270 kHz	
Input sensitivity for 26 db signal-to-noise ratio at 40 kHz deviation	2.6 μV	1.6 μV
Limitation at 75 kHz deviation	1.5 μV	0.85 μV
Output voltage at 40 kHz deviation	290 mV	100 mV

Coil data:

L_1	6 turns	0.15 mm ϕ Cu L center-tap
L_2	5 turns	0.25 mm ϕ Cu L
$L_{1,2}$	on cylindrical core B 61 110 U 17, 2 × 6	
L_3	6 turns	0.8 mm ϕ Cu Ag on core 5 mm ϕ, center-tap
L_4	2 turns	o.5 mm ϕ Cu L, wound into grounded part of L_3
L_6	5 turns	0.8 mm ϕ Cu Ag on core 5 mm ϕ, center-tap

L_5	2 turns	0.5 mm ϕ Cu L, wound into center of L_6
L_7	12 turns	0.25 mm ϕ Cu L
L_8	6 turns	0.25 mm ϕ Cu L
$L_{7,8}$	on Vogt kit D 71-2499.1	
L_9	15 turns	0.25 mm ϕ Cu L
	on Vogt kit D 71-2499.1 without tub-shaped core	
Ferrite bead	B 62 110 M 11 3.5 × 1.2 × 5.2	
SFE 10.7 MA	ceramic filter	

2.9 Increase in variable semiconductor capacitance (ELE-720222)

In Fig. 2.9 the high-frequency signal is fed to the resonant circuit inductance 3 via the coupling winding 2. This functional unit 4 and 6 having a capacitive effect is switched in parallel with the resonant circuit inductance via terminal 1. The supply voltage is applied to point 9.

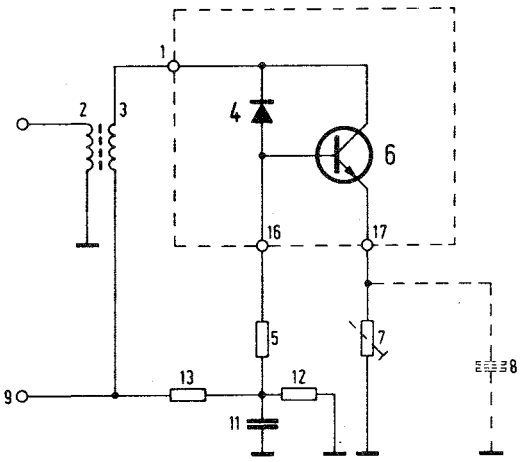


Fig. 2.9

The high-frequency current flowing through tuning diode 4 generates a voltage drop at resistor 5. Its value is much smaller than the capacitive resistance of tuning diode 4 at the resonant frequency, i. e. the phase shift between the voltages on both sides of the tuning diode is almost 90°.

The voltage across resistor 5 controls the current of transistor 6 whose emitter resistor 7 and emitter capacitor 8 determine the operating point and the effective transconductance of the transistor. The collector current of the transistor flows through the resonant circuit. A relatively small reactive current flowing through tuning diode 4 causes a considerably higher current at terminal 1 the phase position of which being in agreement with the phase position of the current through the tuning diode. Thus the entire arrangement, measured at point 1, has a capacitance C_r of

$$C_r = C_D \times (1 + V)$$

In this case, C_D is the tuning diode capacitance and V the current gain of the amplifier in consideration of its external wiring. To keep the resultant quality of the resonant circuit thus formed high the output resistance of the amplifier must be large. Furthermore, the phase error of the current gain must be small. This phase error may be compensated by the capacitor 8 which is shown in dotted lines. Other phase correction elements may also be employed. Through an overcompensation of the phase error the quality of the tuned circuit may also deliberately be increased.

It is surprising that the method of capacitance increase by way of amplification so described is stable also in resonant circuits over the entire frequency range, i. e. that it does not tend towards self-oscillation.

3. TV Circuits

3.1 H-generator and driver (PH-7303-06)

The H-generator presented in Fig. 3.1 allows an easy control of its oscillating frequency at high resistive values via a d. c. voltage. The control current is then very low. It is about 80 µA. The Z-diode BZX 55 C 12 stabilizes the voltage to 12 V and thus indirectly the frequency. The circuit has the following function: The resonant circuit, with the blocked transistor BD 137, starts to produce a sine half-wave in positive direction. The transistor BC 238 is connected through until, with a declining sine voltage across the transformer, the charge voltage at capacitor C_1 will reblock the transistor. Transistor T_2 is thus switched through and the inductor L stores again energy. When transistor 2 is blocked the sine half-wave starts to rise again. Capacitor C_2 permits a rise of the fly-back voltage to only approximately 60 to 80 V. A corresponding puncture-proof type is to be chosen (BD 137 or BD 139 at $V_B = 30$ V).

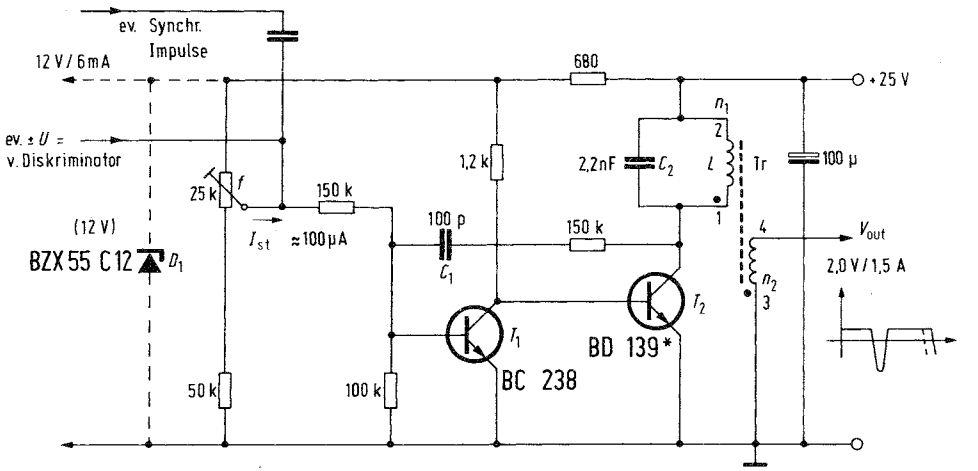


Fig. 3.1

This H-generator may be termed a combination sine-blocking oscillator. It may be synchronized directly both by a phase comparator circuit or narrow positive or negative pulses. Only a few components are required.

Technical data:

V_B = 25 V (12 to 30 V)
I_B = 80 mA
I_{cont} = 80 µA
V_{out} = 2 V
$I_{out\ max}$ = 1.5 A
$R_{o\ min}$ = 1.3 Ω (flow phase)
f = 15,625 Hz ± 1000 Hz (as of $V_B \geqq 10$ V)

Transformer data
EE 20 A 250 Mat. T 26
n_1 = 30 turns 0.35 mm ϕ Cul (center)
n_2 = 300 turns 0.20 mm ϕ Cul (150 turns inside, 150 turns outside)

*) With small sets BC 337 and $V_B \leqq 20$ V (possible change of transformation ratio of transformer Tr required)

3.2 Black/white horizontal deflection circuits for portable TV sets (PH-7303-07)

Compared to "stationary" TV sets portable black/white TV sets with picture sizes of approx. 30 cm diagonal for selective power supply and battery operation make different demands on the circuitry. In future, new concepts of technology and circuitry will find every increasing acceptance — above all when they entail economical, technical and, in part, also mechanical advantages. Work on triple-diffused transistors have progressed in the Siemens Semiconductor Division so far that a number of new design concepts may be discussed. Because of battery operation, the portable TV sets have to work with the socalled low-voltage circuit. In case of power supply operation, the mains voltage has to be transformed to the battery voltage. This is done conventionally with a transformer and a series regulated power supply which may also be used for battery operation.

A good picture quality (width stability) may thus easily be obtained. The triple diffused transistors BU 310, 311 and 312 and the deflection diodes SSi C 4610, SSi C 4620 and SSi B 2520 B are especially suitable for such horizontal deflection output stages. The series regulated power supply may be transistorized with BD 434 to BD 442 and BD 533 to BD 538.

In case of mains operation, a switch-mode power supply may be used besides the well known 50 Hz method. In this case a 15 to 20 kHz ferrite transformer will be employed. The most economical TV power supply is probably that one using the line transformer as a mains transformer at the same time (Siemens pump deflection circuit). A second ferrite transformer similar to a line transformer thus becomes superfluous. The transistor BU 111 is particularly suitable for this circuit. If preference is given to supply voltages of 16 to 24 V and yet battery operation on 12 V must be ensured a booster diode must be used to raise the voltage. The suitable types here are high-speed diodes SSi C 3005 to SSi C 3305.

Two circuits are shown in Fig. 3.2.1 and Fig. 3.2.2 below which, in similar form, have found large-scale application in the TV industry.

Fig. 3.2.1 represents the circuit with a possibility of connection to 220 V and, switched over, to a 12 V car battery. There is no "boosting". The TV portable operates directly on the supply voltage of 12 V. The control element provided for supply operation is also used for battery operation.

Fig. 3.2.2 shows a very simple circuit representing, in principle, the original form of the Siemens pump deflection circuit. The voltage of 18 V is automatically derived from the circuit. In case of battery operation, the voltage is boosted from 12 to 18 V, by means of diode D_3. The starting voltage for the H-generator and the pump circuit is derived from the capacitive division at the supply input C_1, C_2. When the full voltage is supplied the diode D_1 separates the supply voltage from the now lower divided d.c. mains voltage. The pulse width of the control pulse and thus the 18 V are set by means of the potentiometer P. Any effects of inductance spreads of the switching transistor are thus eliminated within a large range.

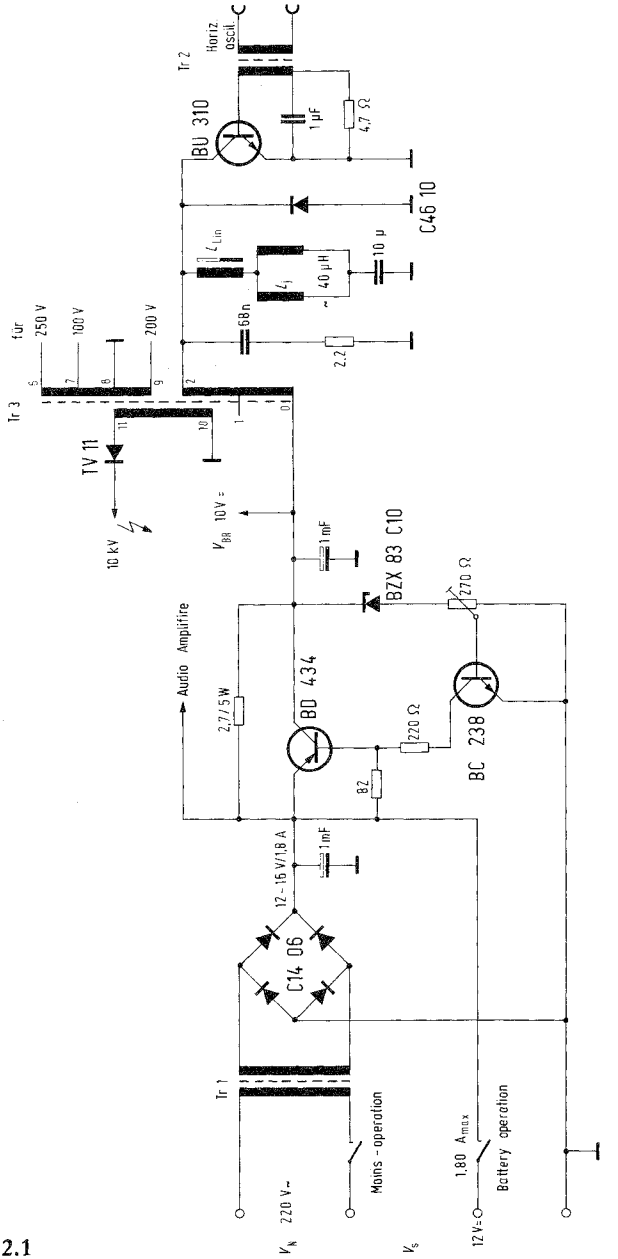

Horiz. oscil.
Tr 2
BU 310
1 µF
4,7 Ω
C46 10
10 µ
68n
2,2
für
250 V
100 V
200 V
Tr 3
TV 11
10 kV
1 mF
BZX 83 C10
270 Ω
Audio Amplifire
2,7/5 W
BD 434
220 Ω
BC 238
82
12 - 15 V/1,8 A
C14 06
Tr 1
220 V~
Mains - operation
1,80 A max
12 V=
Battery operation

Fig. 3.2.1

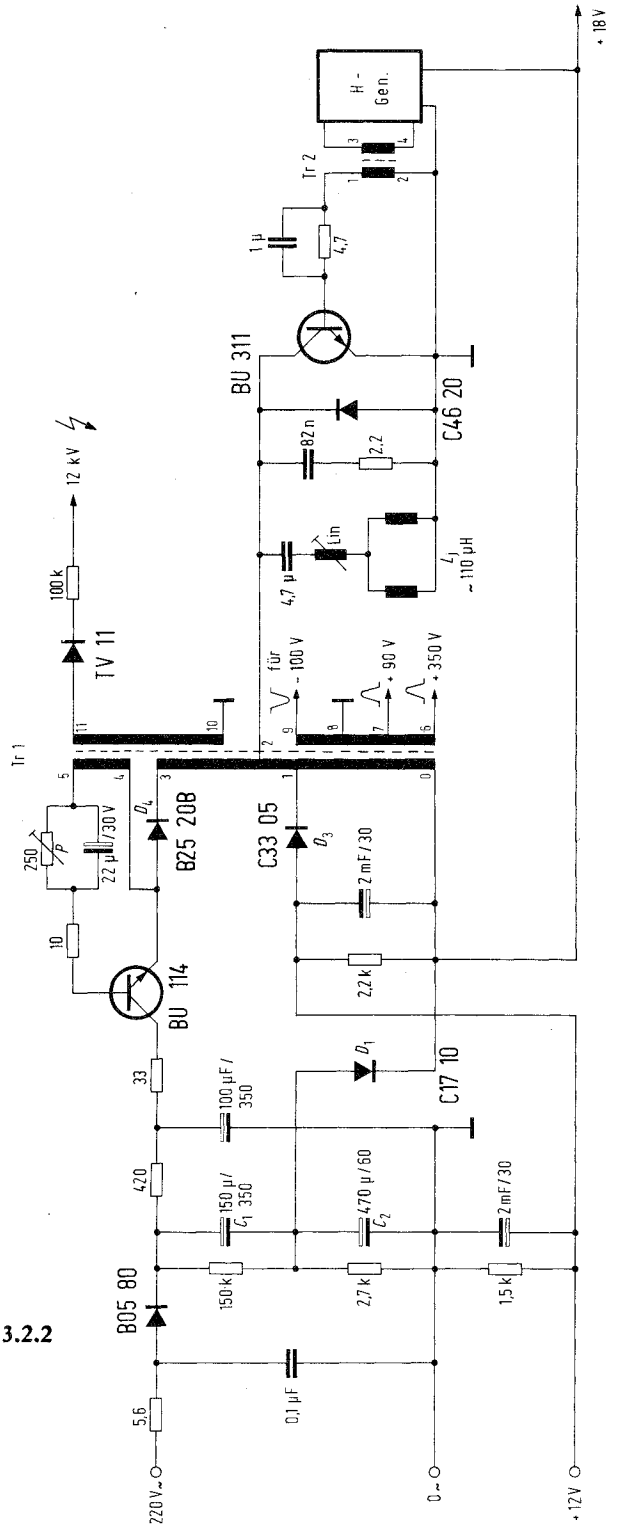

+ 18 V
H-Gen.
Tr 2
1 µ
4,7
BU 311
C46 20
82 n
2,2
4,7 µ
Lin
L_1 ~ 110 µH
12 kV
100 k
TV 11
für - 100 V
+ 90 V
+ 350 V
Tr 1
250
P
22 µ / 30 V
D_4
B25 20B
C33 05
D_3
2 mF / 30
10
BU 114
2,2 k
D_1
C17 10
33
100 µF / 350
420
150 µ / 350
C_1
470 µ / 60
C_2
2 mF / 30
B05 80
150 k
2,7 k
1,5 k
5,6
0,1 µF
220 V~
0~
+ 12 V

Fig. 3.2.2

3.3 Flyback-operated power supply for H-deflection (b/w) (PH-7303-08)

The H-deflection circuit described below has a switch-mode power supply feeding the remaining TV circuitry via the line transformer. The power supply causes an electrical separation from the mains and is controlled in a way that mains and load changes are well balanced. The control and regulating transistors are arranged separately from the power system; the switching transistor only is on the mains side.

Is a voltage applied to the 30-V-terminal shown in Fig. 3.3 the line-deflection transistor BU 110 and its total driving circuits operate in the known conventional manner without the 220 V power supply being connected to the mains (important for service). Troubles in the power supply and the set may thus easily be found. In normal mains operation, transistor TV 146 operates as switching transistor and its control pulse is influenced during the line flyback period with respect to pulse width and pulse phase position. Transistor T_2 (BD 139-10) drives the small pulse transformer Tr_1. Transistor T_1 causes the time control of the driver pulse via the reference diode. With the aid of transistor T_4 the pulse position may be varied from 0 to 2.5 µs. This is sufficient to obtain a good high-tension control.

The Z-diode D_1 separates a part of the transformed flyback pulse (Tr_2 terminal 5-6) and clips it. The C_1-R_1 section differentiates the pulse and feeds a variable triangular pulse to the driver transistor T_2 via the control bias. The current generated by the high tension (0 to 400 µA) controls the collector current at transistor T_4, which shifts the pulse section at the Z-diode D_1 in the same amount up and down thus causing a slight time shift in the used leading edge of the pulse.

The control effect for the high tension is now achieved by the fact that in case of 3-H-tuning the first overshoot will get more or less energy on the primary side and thus a higher or lower high-tension is caused during the pulse peak on the secondary side. When the pulse is now shifted the same energy is fed into the flyback even per line. The obtainable picture stability is excellent as a function of the beam current and mains voltage changes ($\leqq 1$ %).

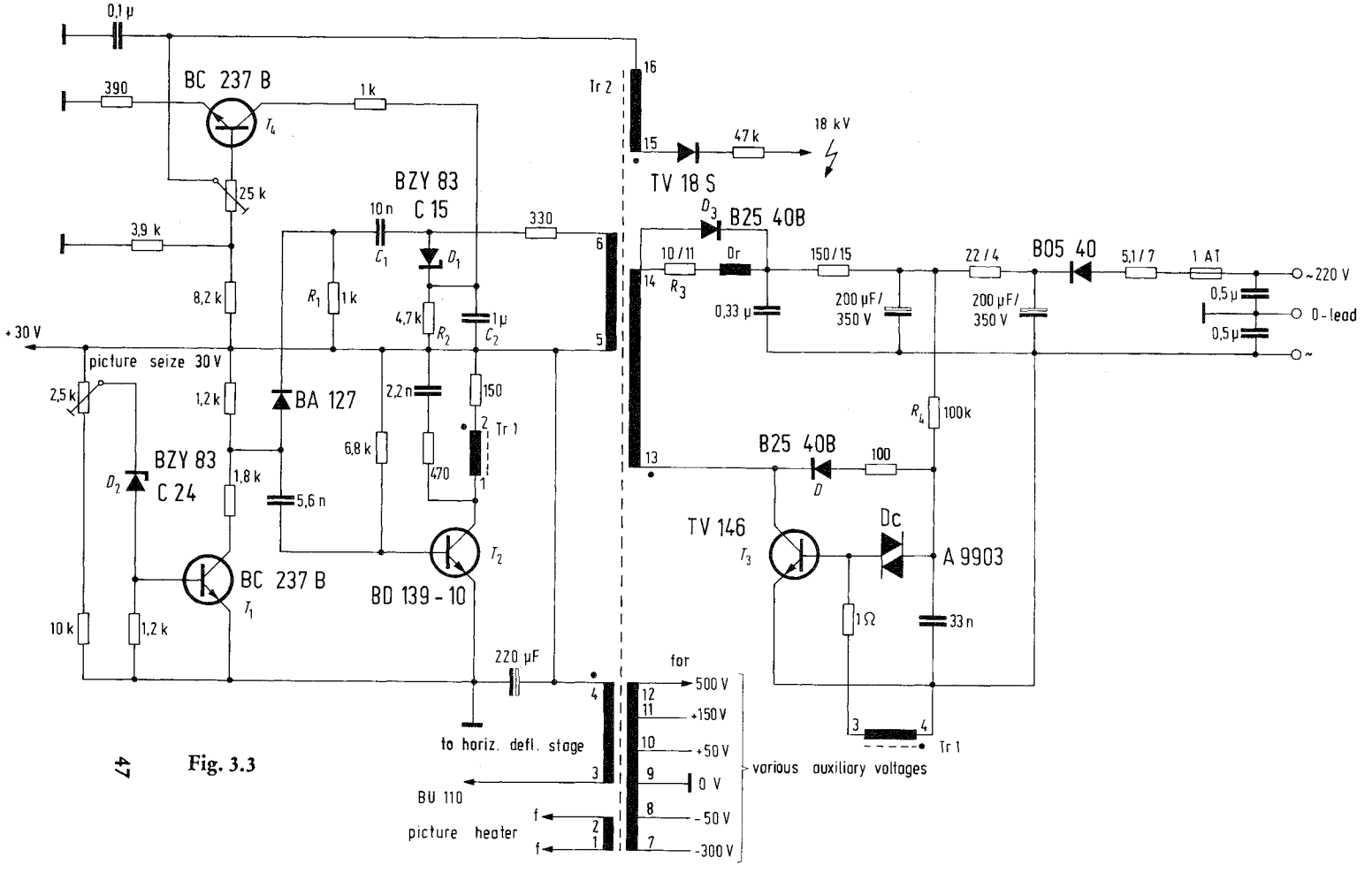

0,1 µ
390
BC 237 B
T_4
1 k
25 k
3,9 k
8,2 k
R_1 1 k
10 n
C_1
C 15
D_1
330
4,7 k
R_2
1 µ
C_2
+ 30 V
picture seize 30 V
2,5 k
1,2 k
BA 127
2,2 n
150
6,8 k
470
Tr 1
BZY 83
C 24
D_2
1,8 k
5,6 n
T_2
BC 237 B
T_1
BD 139 - 10
10 k
1,2 k
220 µF
to horiz. defl. stage
BU 110
picture heater
Tr 2
16
15
47 k
18 kV
TV 18 S
D_3 B25 40B
10 / 11
Dr
R_3
0,33 µ
150 / 15
200 µF / 350 V
22 / 4
200 µF / 350 V
B05 40
5,1 / 7
1 AT
~ 220 V
0,5 µ
0 - lead
0,5 µ
~
R_4 100k
B25 40B
100
D
13
14
TV 146
T_3
Dc
A 9903
1 Ω
33 n
3
4
Tr 1
for
12 500 V
11 +150 V
10 +50 V
9 0 V
8 -50 V
7 -300 V
various auxiliary voltages
6
5
4
3
2
1
f
f

Fig. 3.3

The circuit is started by means of diac A 9903 via the R_4-resistor. In case of low-voltage-short-circuit the choke Dr will protect the transistor T_3 against excessive collector current pulses.

The output stage of the sound section should not influence the picture size. The sound amplifier has to be set to class A or AB operation (constant load). See also Siemens Design Examples of Semiconductor Circuits 1971/72, page 19, chapter 1.5.

Transistor 4 and its wiring may be omitted if the demands on picture stability are not too stringent. The dependence of the picture size on the beam current and mains voltage will be about 2 % in that case.

3.4 H-deflection with medium-voltage transistor BU 212

Any choice of the design concept for a transistorized thin-neck H-deflection circuit must be based on the data of the toroid deflection unit. At 0.31 mH and a deflection current of 11.8 A_{pp} there is a kickback voltage of 610 V_{pp}. As the transistor is to be connected directly to the deflection circuit without any additional transformation, provision was made for the medium-voltage transistor BU 212. This transistor has large safety reserves, for instance, the permissible peak collector current is 17 A while only 9 A are used in the circuit. The total power dissipation P_{tot} is 85 W whereas in the circuit a power dissipation of 5 W is to be expected with a medium transistor. An economical overall concept also entails a simple raster correction circuit. The single transductor raster correction well tested in the 110° standard neck circuit could also be dimensioned to the low ohmic toroid deflection unit. The units involved in the 110°-raster correction are hardly more numerous than in the former 90°-circuits, and the picture quality realized meets standard requirements.

The power supply is of decisive importance to a transistor deflection circuit. For this reason a power supply with blocking oscillator is suggested for use in thin-neck circuits, which corresponds to the circuit used in standard neck methods except for the changed output voltages.

Circuit description

The output stage transistor BU 212 is driven or synchronized by the TBA 920 via the two transistors BC 237 and BD 435. As may be derived from Fig. 3.4, the deflection transistor has no separate diode

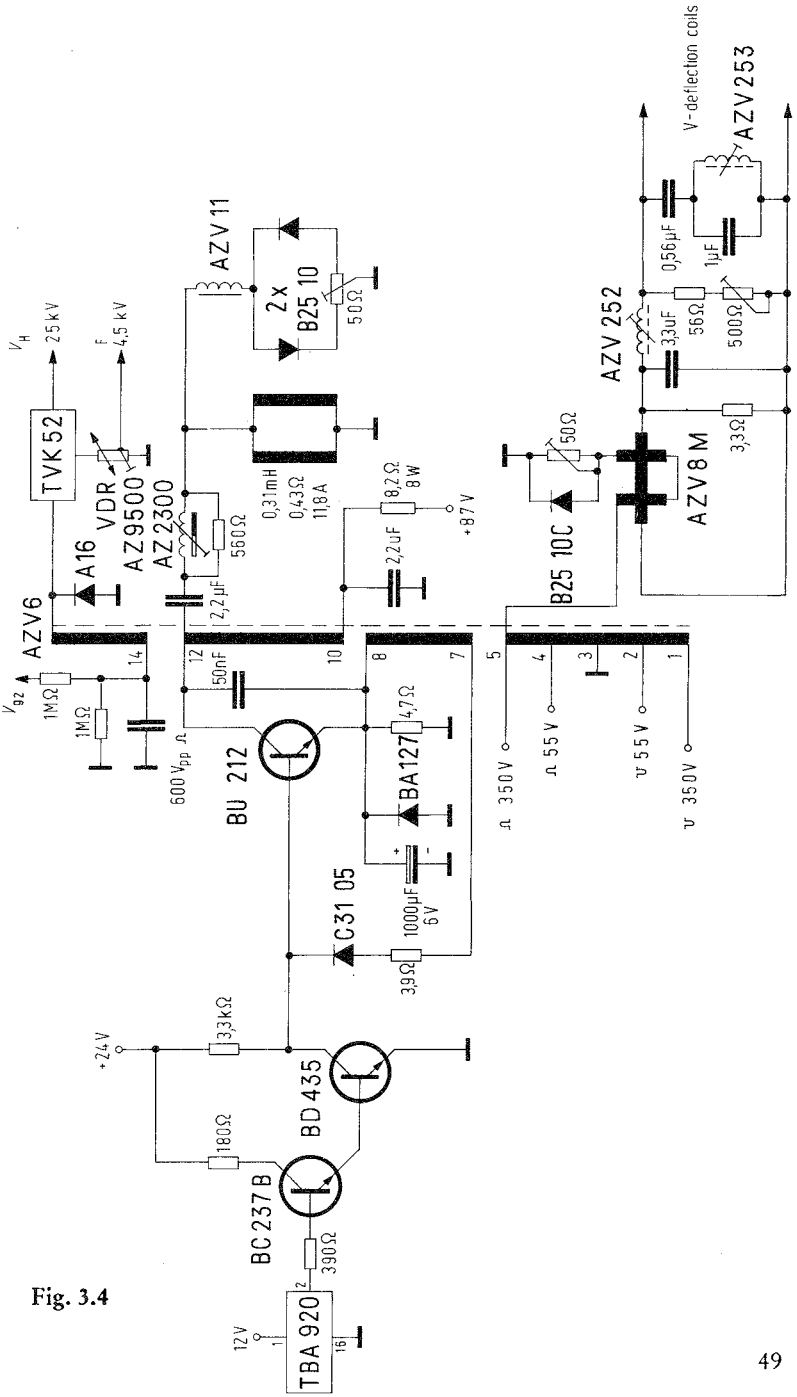

TBA 920
BC 237 B
BD 435
BU 212
BA 127
C31 05
TVK 52
A16
VDR
AZ9500
AZ2300
AZV 11
2x B25 10
AZV6
AZV 252
AZV 253
AZV 8 M
B25 10C
V-deflection coils
12 V
+24 V
+87 V
25 kV
4,5 kV
600 Vpp
350 V
55 V
55 V
350 V
3,3kΩ
180Ω
390Ω
1MΩ
1MΩ
50nF
560Ω
2,2µF
0,31mH
0,43Ω
11,8A
8,2Ω 8W
2,2uF
4,7Ω
1000µF 6V
3,9Ω
50Ω
33uF
56Ω
500Ω
3,3Ω
0,56µF
1µF

Fig. 3.4

for the return current. In our proposed circuit the deflection transistor, during the first part of the sweep, functions according to the principle of the inversely operating collector-base junction. The inverse current then largely flows via the collector-emitter section of transistor BD 435 and a smaller amount via diode C 3105 and the auxiliary winding of the line transformer (terminals 7-8).

The base current for the BU 212 is also taken from this winding.

An important point is the switch-off behaviour at the end of the sweep. In the circuit described the collector current is switched off, with the aid of the emitter-component combination of the BU 212 within 0.6 µs. Due to the arrangement of the diode BA 127 and the 4.7 Ω resistor the emitter potential may be raised during the reverse phase of the BU 212. A considerably steeper switch-off slope may thus be realized.

The transistor BU 212 has a very low saturation voltage of approximately 1 V only.

The high tension is generated by an electrically separated winding of the line transformer and by the cascade. The screen grid voltage V_2 for the picture tube is picked off by diode A 16 at the base of this winding.

This circuit operates without any special protective components for the BU 212. The relatively large safety reserves of the collector current and the collector voltage ensure good protection for high-tension spark-overs. In addition, the dropping resistor of 8.2 Ω and the 2.2 µf capacitor as well as the internal resistance of the power supply will protect the output stage against any such defects. The circuit dimensions were chosen in a way that there will be no overloading of the output stage transistor in case of a missing drive pulse or a missing supply voltage for the prestages.

3.5 H-deflection with BU 208 for 110° standard-neck picture tube (KE-730105)

The standard-neck picture tube A 66-140 X together with the deflection system AT 1062 represents a fairly good compromise as regards purity of colour, convergence and deflection sensitivity. This system requires a H-fly-back voltage of 1250 V so that the 1500 V transistor BU 208 may be directly connected. With the aid of a simple current-limiting

protection switching off the H-output-stage within a few microseconds a high degree of safety is achieved also in case of picture-tube sparkovers and of self-curing operations in the cascade capacitors.

The entire circuitry is particularly simple as there are no reverse current diode and driver transformer. The circuit is arranged in a way that the picture width will change by less than 1 % in case of brightness variations even with a standard selenium cascade.

As may be seen in Fig. 3.5, the BU 208 is operated in common base circuit and controlled directly via the emitter. In this way, it may be switched through and off precisely.

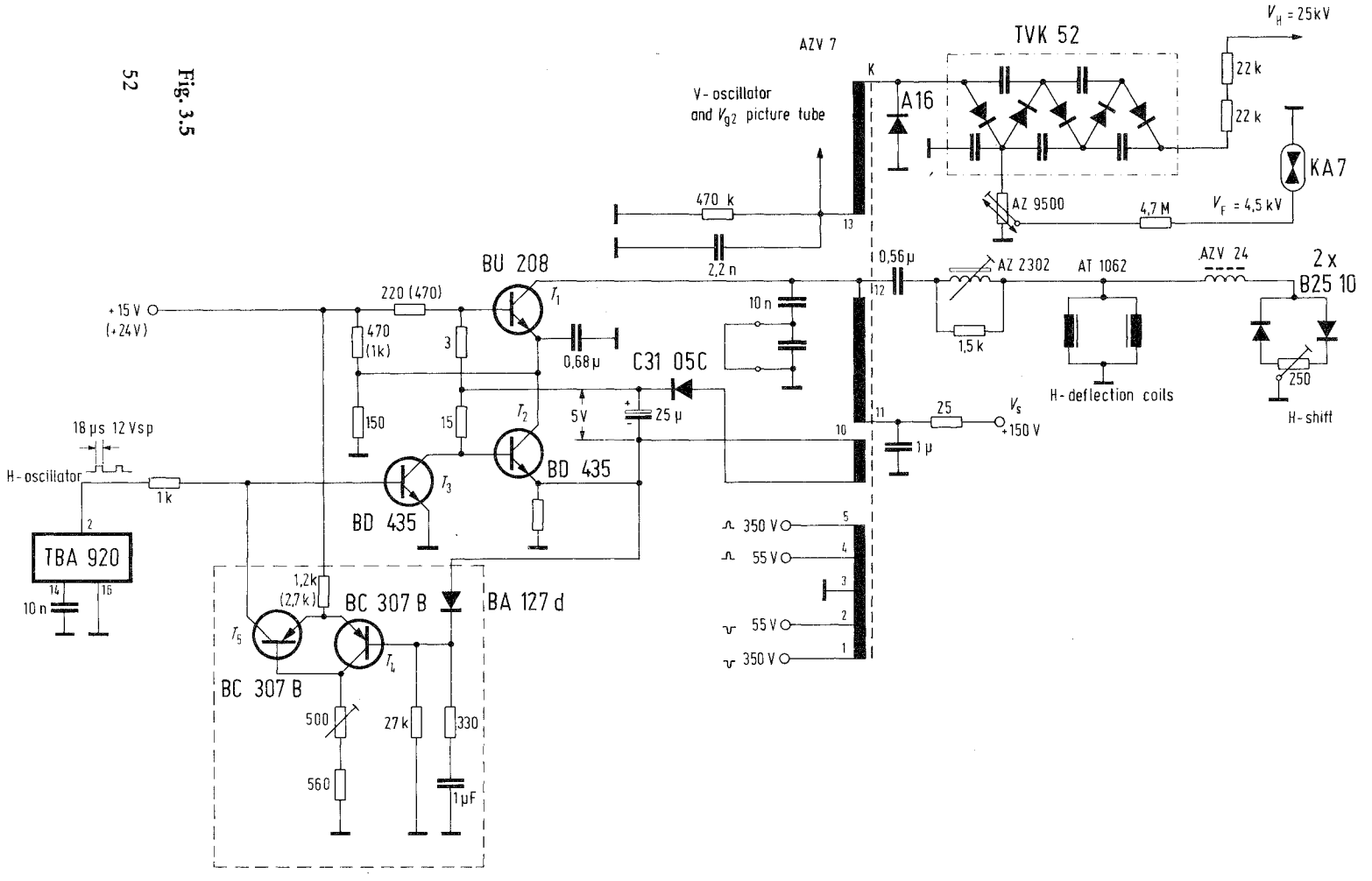
The positive triggering pulse from TBA 920 will turn on the transistor T_3 which has been reversed till then. Up to that moment the transistor T_2 was conductive because it had a positive base voltage from the auxiliary voltage + 5 V via the 15 Ω resistor. The transistor T_2 is reversed and the emitter of BU 208 is thus open. The collector current of the BU 208 now flows as switch-off base current via the 3 Ω resistor, the capacitor 25 µf and the 1 Ω resistor to ground. This switch-off operation lasts for about 3 µs and the BU 208 will then be turned off with a fall time of approximately 0.7 µs. The capacitor 0.68 µf which is switched to ground by the emitter of BU 208 ensures a clean switch-off operation.

After switching on the set, the base current of BU 208 flows from + 24 V terminal (+ 15 V) via resistor 470 Ω (220 Ω) and then from the terminal of the 5 Volt auxiliary voltage supply via resistor 3 Ω. The epibase transistor BD 435 in plastic package SOT 32 is particularly suited as emitter loading transistor T_2 because it will switch through at 4 A with a very low residual voltage of 1 V.

Protective circuit

A special feature of this circuit is the protective circuit consisting of transistors T_4 and T_5. In accordance with the collector current of BU 208 a saw-tooth voltage with a positive peak of approximately 4 V is produced at the 1 Ω emitter resistor. With the adjustable 500 Ω resistor a voltage threshold of, for instance 5 V, is set as a "protective level". If the peak current of the output stage exceeds this protective level of 5 A (corresponding to 5 V) the transistor T_4 which so far has been conducting is reversed and T_5 is switched on. Thus also T_3 is turned on and the transistors T_2 and T_1 are switched off like in a line flyback.

Fig. 3.5


V_H = 25kV
AZV 7
TVK 52
V- oscillator
and V_{g2} picture tube
K
A16
22 k
22 k
KA7
AZ 9500
4,7 M
V_F = 4,5 kV
470 k
13
2,2 n
BU 208
T_1
0,56 µ
AZ 2302
AT 1062
AZV 24
2 x
B25 10
220 (470)
+15 V
(+24 V)
470
(1k)
3
10 n
12
1,5 k
H- deflection coils
250
H- shift
0,68 µ
C31 05C
150
15
T_2
5V
25 µ
11
25
V_s
+150 V
18 µs 12 Vsp
H- oscillator
1 k
T_3
BD 435
BD 435
10
1 µ
350 V
5
55 V
4
3
55 V
2
350 V
1
2
TBA 920
14
16
10 n
1,2k
(2,7 k)
BC 307 B
BA 127 d
T_5
T_4
BC 307 B
500
27 k
330
560
1µF

They are automatically switched on again after a few milliseconds as soon as the capacitor of 1 µf has discharged at the base of transistor T_4 via the 27 kΩ resistor. In case the trouble that has caused the increased collector current of the output stage (e.g. a short-circuit in the transformer or of the high-tension) prevails the protective circuit will again switch off the output stage at 5 A and tries to switch the output stage on again with a repetition frequency of approximately 300 Hz. In case of protective circuit operation, the current consumption of the output stage drops almost to zero. Protection is granted against: picture tube spark-overs, short-circuits in transformer and at transformer outputs, overload through excessive beam current, increase in the operating voltage due to defects in the power supply, drift of the H-oscillator towards lower frequencies, interruption or short-circuit of the H-oscillator, interruption of the cable to the deflection unit.

Measuring results of the H-output stage:

Beam current	I_B	0	0.1	1.2	1.5	mA
Operating voltage		150	150	150	150	V
DC voltage at H-transformer pt 11		139.0	138.5	133.0	131.0	V
Current-consumption	I_g	500	530	690	750	mA
High-tension	V_n	25.0	24.9	22.6	22.0	kV
Picture width	B	100	100.6	101.4	101.4	%
Flyback voltage at H-yoke	V_J	1.4	1.4	1.3	1.35	kV
Flyback time	t_r	10.0	10.0	10.1	10.1	µs
Deflection current	I_{def}	6.2	6.2	6.1	6.0	A
Internal resistance	R_i	2.0	2.0	2.0	2.0	MΩ
BU 208						
Collector peak current	$+I_{cp}$	4.4	4.4	4.4	4.4	A
Inverse collector peak current	$-I_{cp}$	3.4	3.4	3.2	3.0	A
Collector peak voltage	V_{cp}	1.3	1.3	1.25	1.22	kV
Collector power dissipation	P_c		3 to 8*			
Storage time	t_s	3.5	3.5	3.3	3.2	µs
Fall time	t_f		0.5 to 2*			

*) Depending on gain B, switching time and temperature of BU 208

Measuring results at transistor BD 435

Collector peak current	$+I_{cp}$	5.2	5.2	5.2	5.2 V
Inverse collector peak current	$-I_{cp}$	1.2	1.2	1.0	1.0 A
Collector peak voltage	V_{CEp}	18.0	18.0	17.0	17.0 V

3.6 Blocking oscillator power supply 220 V for colour TV sets (KE-7301)

The power supply of a fully transistorized colour TV set must be able to deliver power in the amount of approximate 180 W, which is composed as follows:

Picture tube heating about	6 W
H-output stage	70–95 W
Video and colour output stages about	25 W
Low-voltage stages about	60 W

Of course, considerable variations are feasible, depending upon the design of the set. However, the total power will in any case probably remain below 200 W. A "full performance" power supply should meet the following requirements:

Mains voltage variations of ± 15 % should be controlled to ± 1.5 %.

Load variations between 70 and 95 W at the 150-V-output caused by brightness changes should have a very low influence on the other voltages (voltage changes max. 1.5 %).

The mains hum of 15 V_{pp} at the input should be controlled to less than 0.5 V_{pp}.

All outputs should be resistant to short-circuit and overload. After having switched off short-circuit or overload the power supply should continue to operate. Also under no-load conditions the power supply should be reliable because this state may occur during manufacture or service.

The requirements made may be realized in a very simple and economical manner by means of a blocking oscillator (**Fig. 3.6**).

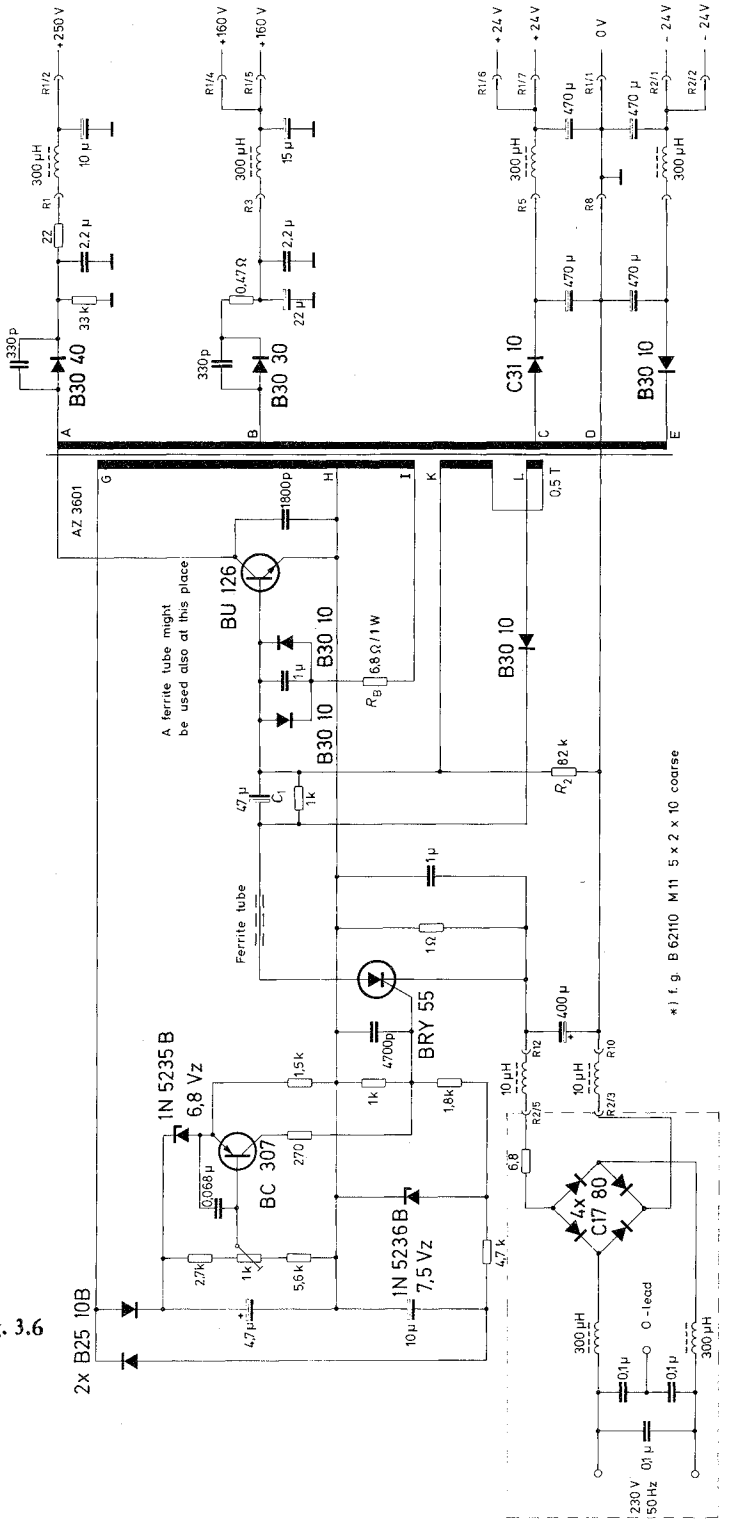

+250 V
+160 V
+160 V
+24 V
+24 V
0 V
-24 V
-24 V
R1/2
R1/4
R1/5
R1/6
R1/7
R1/1
R2/1
R2/2
300 µH
10 µ
15 µ
470 µ
2.2 µ
33 k
0,47 Ω
22 µ
330 p
B30 40
B30 30
C31 10
B30 10
A
B
C
D
E
AZ 3601
G
H
I
K
L
0,5 T
1800p
BU 126
1 µ
6,8 Ω / 1 W
B30 10
82 k
47 µ
1 k
1 µ
1 Ω
Ferrite tube
A ferrite tube might be used also at this place
400 µ
10 µH
1,5 k
4700p
BRY 55
1,8 k
1N 5235 B
6,8 Vz
BC 307
270
0,068 µ
2,7 k
5,6 k
1N 5236 B
7,5 Vz
4,7 k
10 µ
4,7 µ
6,8
4x
C17 80
2x B25 10B
0 - lead
0,1 µ
230 V
50 Hz
*) f. g. B 62110 M11 5 x 2 x 10 coarse

Fig. 3.6

The mains AC voltage is rectified with the aid of a bridge circuit consisting of 4 silicon rectifiers C 1780 and smoothed with a 400 µf electrolytic capacitor. BU 126 serves as switching transistor. Transformer AZ 3601 only has one ferrite core of size EE 42 because it operates as an autotransformer. It has good coupling properties and offers an almost rectangular collector voltage with a very low overshoot only.

The circuit is not synchronized with the line frequency but oscillates in case of full load to approx. 18 kHz and in case of 60 % load to approx. 25 kHz. In practice, the frequency in a TV set fluctuates between 18 and 22 kHz. On open-circuit operation, the blocking oscillator circuit changes to a stable sine-wave operation with approx. 50 kHz. The circuit may easily control mains voltage variations of ± 20 %, the duty cycle changes accordingly.

In contrast to synchronized switch-mode power supplies requiring a very complicated regulating circuit this self oscillating power supply operates with a very simple control circuit. The diode D_1 produces a reference DC voltage of + 24 V. This voltage is proportional to the other output voltages of the circuit (+ 250 V, + 150 V, + 24 V, etc.) due to the good coupling of the transformer. The transistor BC 307 compares part of this reference voltage in the known manner with the stabilized voltage across the Z-diode and simultaneously serves as a AGC amplifier. The thyristor BRY 55 is fired via the anode gate. The firing depends both on the AGC voltage of the transistor BC 307 and the voltage drop across the 1 Ω resistor R_1 in the emitter circuit of the transistor BU 126 which is proportional to the saw-tooth collector current. Only during the switch-off time of the switching transistor the thyristor is switched on.

The thyristor is turned off during the inverse period of the switching transistor because during this period the feedback voltage across the base of BU 126 and thus across the anode of BRY 55 becomes more negative than the cathode.

The switching transistor BU 126 oscillates with a feedback voltage which is tapped at the transformer terminals H and I. When the thyristor is turned on the base of BU 126 is grounded and the feedback is shorted. Thus the DC voltage of 4 V across the capacitor C_1 becomes effective as a reverse voltage and the switching transistor is turned off with a switch-off time of approx. 2 µs and a fall time of 0.6 µs. The control principle is thus based on a shifting of the switch-off point.

The resistor R_2 is used as an initial resistance. During the starting operation the circuit oscillates by its own feedback until the reference voltage of 24 V is built up so that control operates and stabilizes the voltage.

The function of this circuit may thus be termed a "self oscillating reverse-voltage transformer with a triggered disconnection". This type of turn-off ensures favourable switching characteristics.

The blocking oscillator power supply described may also further be developed for 110 V or, switchable, for 110/220 V.

3.7 Line deflection and high-voltage circuits with thyristors

Thyristor deflection circuits (Fig. 3.7.1 and 3.7.2) for horizontal deflection with high-voltage generation are used in black/white or colour TV sets. In principle they consist of three resonant circuits set into operation one after the other.

1) The sweep circuit consists of the closed sweep switch (thyristor and diode) and the effective inductance made up of H-transformer with H-deflection coil and of the series-connected capacitor. The latter determines the shape of the deflection current during the sweep in joint action with the field linearity control.

2) The commutating circuit is closed shortly before the end of the sweep by a pulse of the H-oscillator. It introduces the flyback by switching off the sweep switch through the commutating current. Therefore we have the following circuit: closed flyback, switch, commutating coil, balancing coil, capacitor-T-section, closed sweep switch.

3) When sweep thyristor and diode are no longer conducting we have the following kickback resonant circuit: flyback switch, commutating coil with balancing coil, capacitor-T-section, inductance made up of line transformer and deflection coil, series capacitor.

In addition to this resonant circuit, there is another one compensating for the losses incurred and supplying more and less energy in case of load and mains variations. It thus achieves that a constant pulse voltage is being applied to the sweep switch.

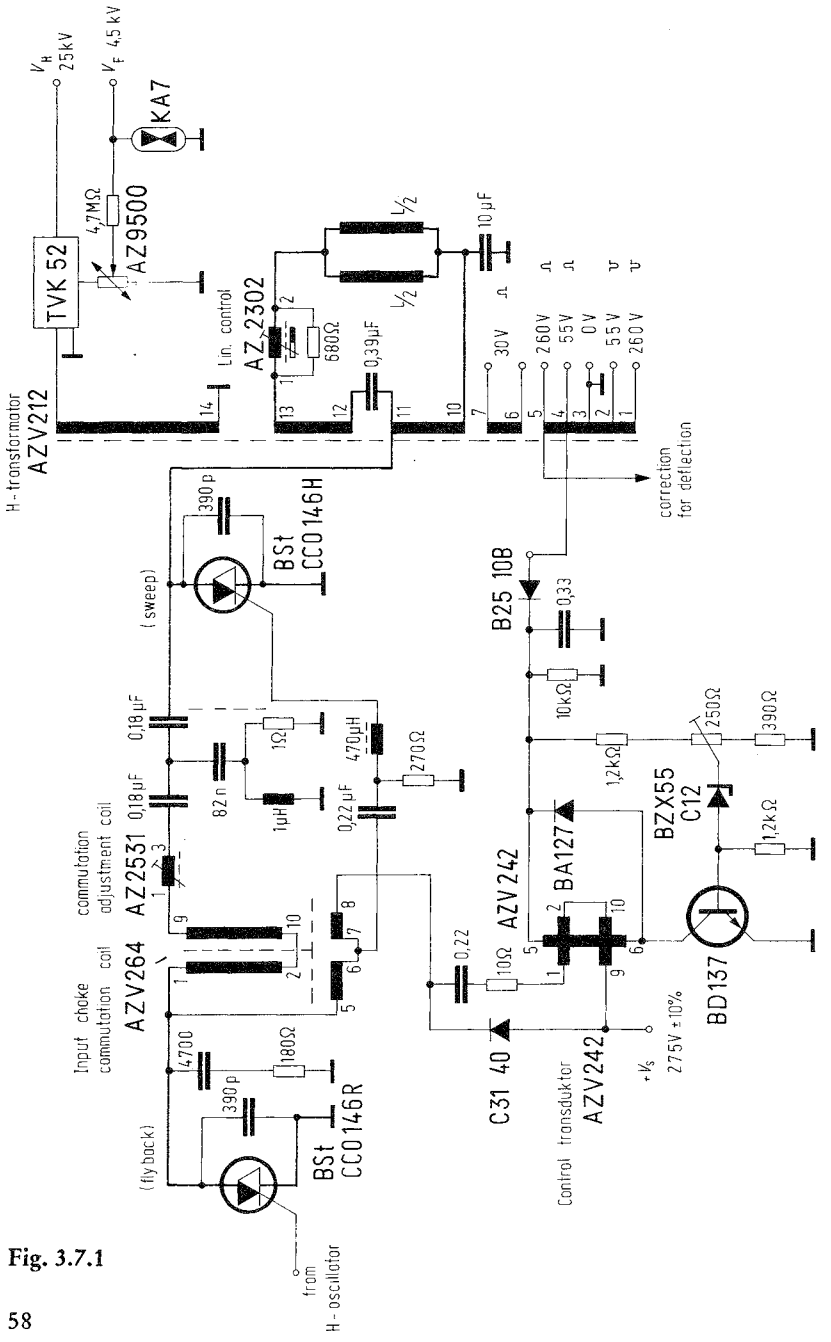

H-transformator
AZV212
TVK 52
V_H 25kV
V_F 4,5 kV
KA7
4,7MΩ
AZ9500
Lin. control
AZ 2302
680Ω
0,39µF
½
½
10 µF
30 V
260 V
55 V
0 V
55 V
260 V
correction for deflection
B25 10B
0,33
10kΩ
1,2kΩ
250Ω
390Ω
1,2kΩ
BZX55 C12
BD137
BA127
AZV242
Control transductor
AZV242
C31 40
10Ω
0,22
+Vs
275V ±10%
AZV264
Input choke commutation coil
commutation adjustment coil
AZ2531
0,18µF
0,18µF
82n
1Ω
1µH
470µH
0,22µF
270Ω
BSt CCO146H
(sweep)
390p
BSt CCO146R
(fly back)
4700
180Ω
390p
from H-oscillator

Fig. 3.7.1

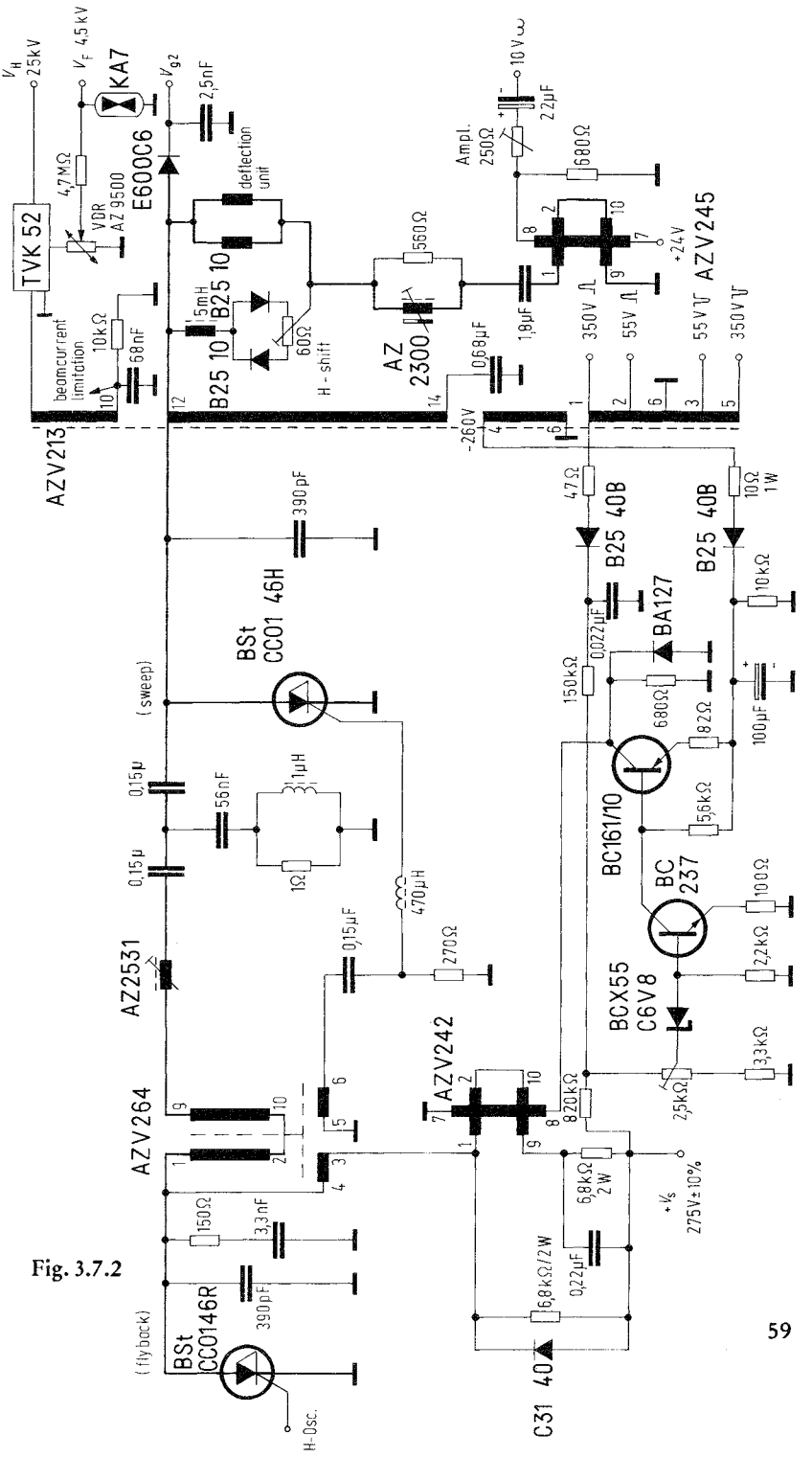

AZV213
AZV264
AZ2531
AZV242
AZV245
TVK 52
KA7
E600C6
AZ 2300
BSt CC01 46H
BSt CC0146R
BC161/10
BC 237
BCX55 C6V8
B25 40B
C31 40
BA127
deflection unit
H-shift
H-Osc.
(sweep)
(flyback)
beamcurrent limitation
Ampl.
VDR AZ 9500
+24 V
+½ 275V±10%
-260V
25kV
4,5kV
10Vss
350V
55V
55V
350V

Fig. 3.7.2

This circuit is closed via the operating voltage, control transductor, input choke, commutating coils, capacitors and sweep switch. The resonant circuit only exists while the sweep switch is closed and the flyback switch is still open. When the flyback thyristor becomes conductive through the H-oscillator, the resonant circuit is interrupted. The load condition of the capacitor-T-section at this moment determines the quantity of energy additionally fed into the deflection circuit during the following kickback operation. This charging operation of the capacitors is influenced by the variable inductance of the control transductor. The latter receives its control information through a pulse at the line transformer.

The following points should be stressed in the design and construction of a deflection circuit:

The specified minimum recovery times for thyristors must be kept.

High peak currents (up to 12 A_p) will occur in the commutating circuit. This fact must be taken into account when choosing the capacitors.

The power generated in the thyristors and diodes must be dissipated by a cooling plate.

The minimum clearance from the neighbouring component specified in the data sheet for the tripler cascade TVK 52 must be observed.

Scatter fields will be caused by the air gap near the commutating coil and input choke. Adequate clearances to other magnetic components should therefore be kept.

The component tolerances should be kept as low as possible, especially those for the capacitors in the T-section. Residual tolerances may be compensated through the variable inductance of the commutating balancing coil.

The circuit diagrams presented show examples of a thyristor line deflection with high-voltage generation. In these cases, an extreme stability of picture width and of high voltage is obtained with load and mains variations. Moreover, the circuits are designed in a way that the energy for other supplies in the colour TV set (e.g. vertical, convergence, IF, raster correction, video) may be derived from the auxiliary coils.

Test data	Standard neck tube (Fig. 3.7.1)	Thin neck tube (Fig. 3.7.2)
Mains voltage in case of half-wave rectification with C 1780	220 V ± 10 %	220 V ± 10 %
Operating voltage for output stage	275 V, uncontrolled	275 V, uncontrolled
Inductance of H-deflection coils	1.1 mH	0.31 mH
Deflection current	6.6 A_{pp}	12 A_{pp}
Deflection voltage (kickback)	1200 V_{pp}	680 V_{pp}
Internal resistance of high-voltage source	approx. 1.5 MΩ	approx. 1.5 MΩ
High-voltage	25 kV	25 kV
Beam current, max.	1.5 mA	1.5 mA
Auxiliary pulse voltages for supplies:	± 55 V_{pp} ± 260 V_{pp}	± 55 V_{pp} ± 350 V_{pp}

3.8 TV-signal sync generator (FB-46-01)

The sync generator (Fig. 3.8.1 and 3.8.2) is used to synchronize TV cameras, flying-spot scanners and test signal generators. All signals are generated digitally. A crystal oscillator serves as sync source. It oscillates at 20 times the line frequency (312.5 kHz). Double the line frequency is produced in a decade divider (FLJ 161). The decoder FLH 281 supplies the various pulse sequences for the generation of sync pulses. Another divider FLJ 161 divides the double line frequency both by two and by five. Thus the line frequency is produced, on the one hand, and a switching signal for the pre- and postequalizing pulses and the wide V-sync pulses on the other hand. The other divider chain (FLJ 161, FLJ 181) serves to generate the frame frequency. To this end, the double line frequency in the CCIR standard has to be divided by 625 and in the FCC standard by 525. As a division by 5 has already been carried out a further counter is required which may be switched over for a dividing ratio of 125 to 105. The switch-over is done by selecting (FLH 101) suitable clear pulses from a decoder FLH 281. A further decoder FLH 281 is used to generate gate pulses for the equalizing pulses and V-pulses. The sync signal mixture S is combined in two gate circuits FLH 101 and FLH 111.

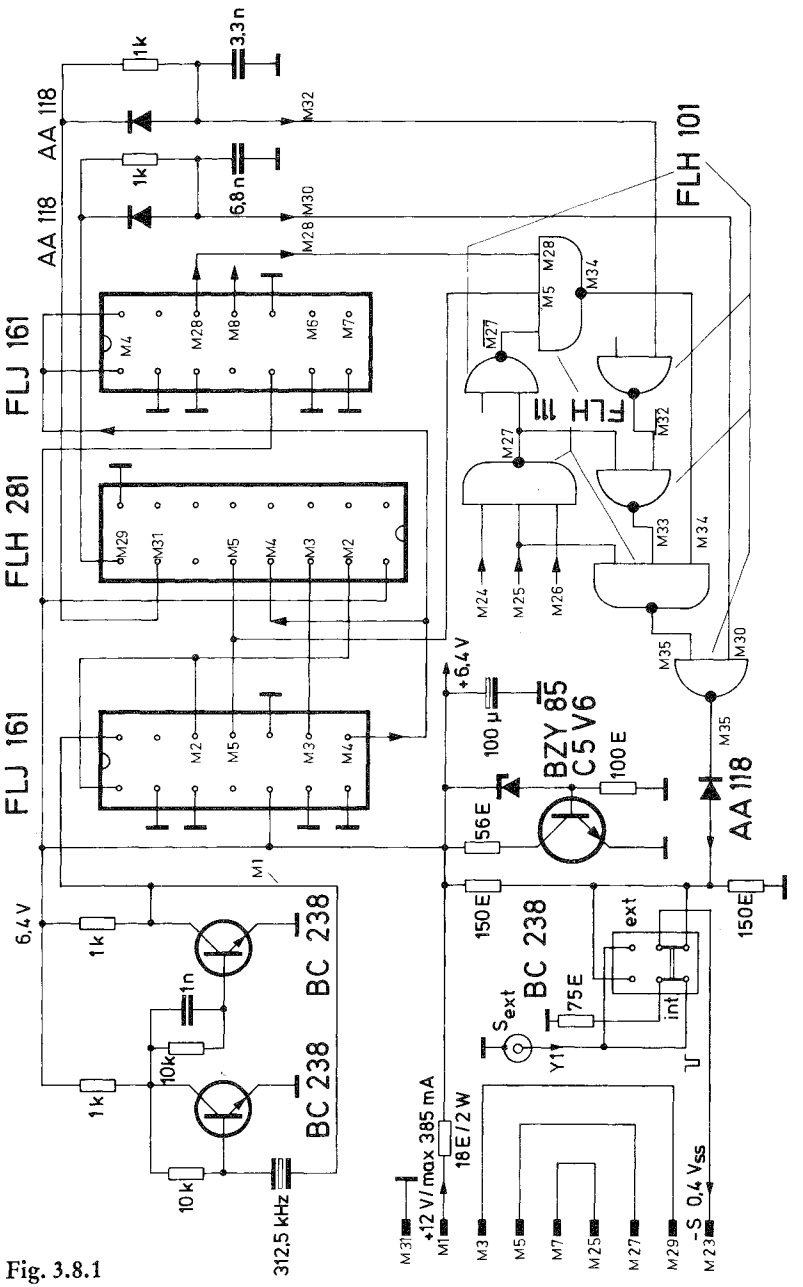

FLJ 161
FLH 281
FLJ 161
AA 118
AA 118
FLH 101
1k
3.3n
6,8n
M32
M30
M28
M4
M28
M8
M6
M7
M29
M31
M5
M4
M3
M2
M2
M5
M3
M4
M1
M27
M5
M28
M34
M32
M33
M34
M24
M25
M26
M35
M30
+6,4 V
100 µ
BZY 85
C5 V6
100 E
56 E
AA 118
M35
150E
150E
6,4 V
1k
1n
10k
1k
1k
10 k
BC 238
BC 238
BC 238
312,5 kHz
S ext
75E
Y11
ext
int
+12 V/max 385 mA
18E/2 W
M31
M1
M3
M5
M7
M25
M27
M29
-S 0,4 Vss
M23

Fig. 3.8.1

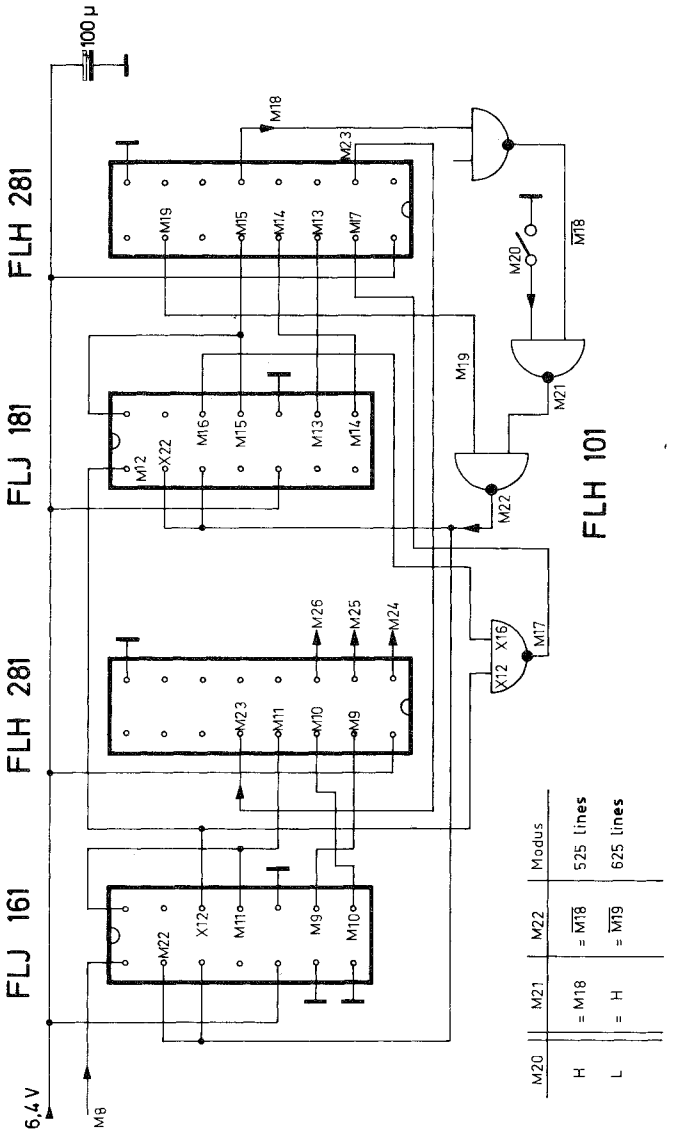

100 µ
FLH 281
FLJ 181
FLH 281
FLJ 161
FLH 101
+6,4 V
M8
M18
M23
M19
M15
M14
M13
M17
M20
M18
M19
M21
M12
X22
M16
M15
M13
M14
M22
M26
M25
M24
M23
M11
M10
M9
X12
X16
M17
M22
X12
M11
M9
M10
M20
M21
M22
Modus
H
= M18
= M18
525 lines
L
= H
= M19
625 lines

Fig. 3.8.2

Only + 6.4 V is required as an operating voltage. In systems having only + 12 V at their disposal, a dropping resistor and a simple stabilizer are provided for. External S signals may be fed into a system by a change-over switch.
Blanking as well as H- and V-pulses may be derived with an additional gate circuit.

Technical data

V_{X1}	Operating voltage	+ 12 V
$\Delta V_{X1}/V_{X1}$	Operating voltage tolerance	± 10 %
I_{X1}	Current consumption	max. 385 mA[2])
V_{X23}	Sync pulse output	— 0.4 V_{pp}[1])
R_{X23}	Internal resistance	75 Ω
V_{Y1}	Sync pulse input	max. 4 V_{pp}
R_{Y1}	Input resistance	75 Ω
$f_{H\ CCIR}$	Line frequency	15625 Hz
$\Delta f_H/f_H$	Tolerance	$< 10^{-4}$
z_{CCIR}	Number of lines CCIR	625
z_{FCC}	Number of lines FCC	525
$f_{V\ CCIR}$	Frame frequency CCIR	50 Hz
$f_{V\ FCC}$	Frame frequency FCC	59.53 Hz
n	Number of frames per picture	2
p_1	Number of preequalizing pulses	5
p_2	Number of postequalizing pulses	5
p_3	Number of V-pulses	5
t_S	Sync pulse duration	4.8 µs
t_T	Equalizing pulse duration	3.2 µs
t_V	V-pulse duration	28.8 µs
t_R	Rise time	max. 30 ns
t_F	Fall time	max. 30 ns

3.9 TV colour bar generator (FB 41-02)

Various test signals are required for device and service of TV sets, video recorders, transmission and control equipment.

---

[1]) at 75 Ω
[2]) V_{X1} = 13 V

The unit shown in **Figs. 3.9.1** and **3.9.2** supplies a colour bar pattern with which to check, in particular, video amplifiers and colour matrix circuits. The pattern is formed by the three signals YAS, R-Y and B-Y. The signal generator represents an independent serviceable unit. All signals are produced digitally.

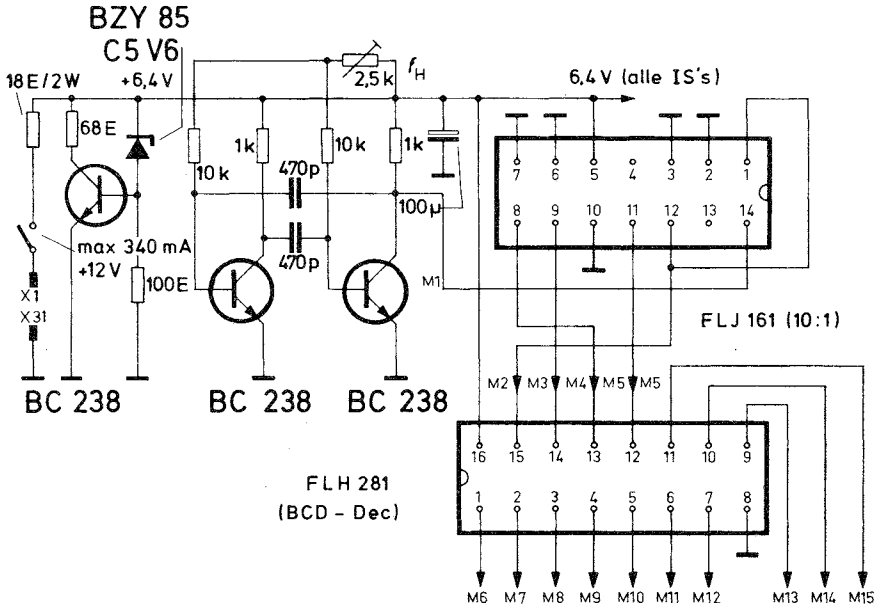


Fig. 3.9.1

A multivibrator oscillating with 10 times the line frequency (156.25 kHz) is used as clock generator. The line frequency is produced by a (10 : 1) – divider FLJ 161. The last three divider stages supply the primary R, G, B signals. The synchronizing pulses and an additional white pulse are generated by the decoder FLH 281. A gate circuit FLH 101 serves to blank the signals. A hex-inverter FLH 211 brings the

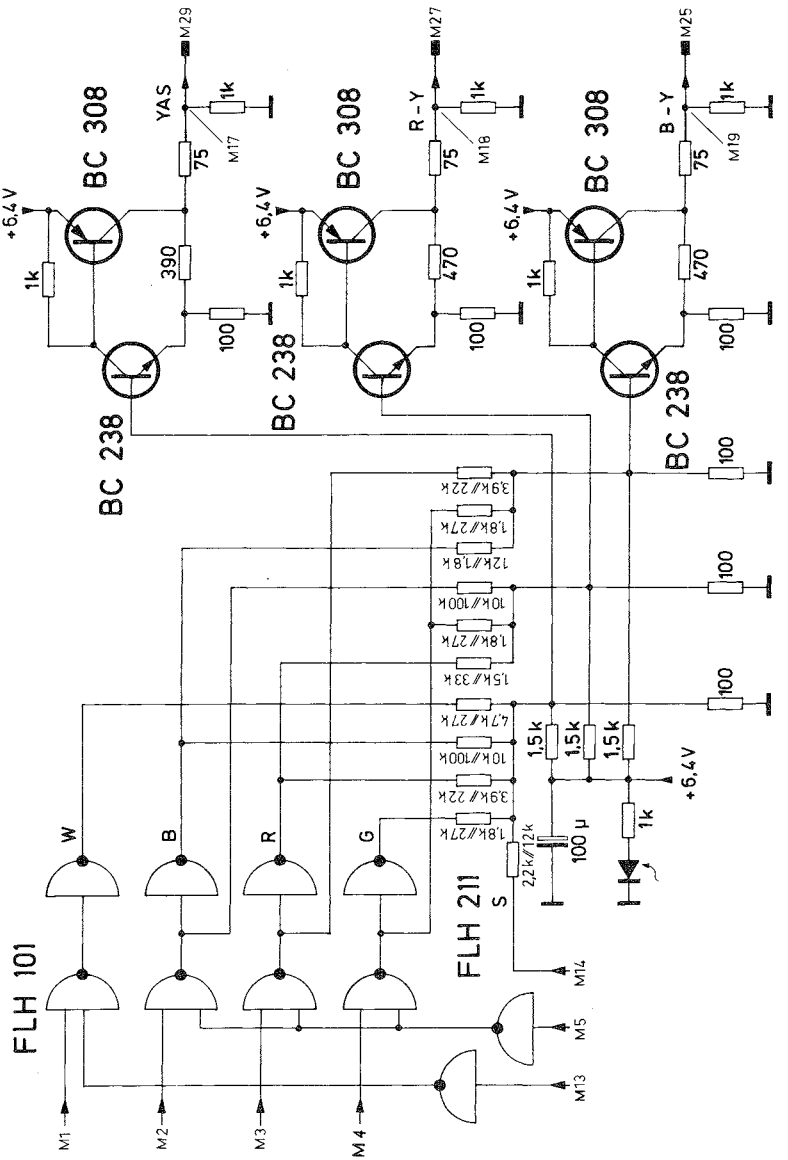

FLH 101
FLH 211
BC 308
BC 238
YAS
R-Y
B-Y
+6,4 V
W
B
R
G
S
M1
M2
M3
M4
M5
M13
M14
M17
M18
M19
M25
M27
M29
1k
75
390
470
100
1,5k
100 µ
2,2k//12k
3,9k//22k
1,8k//27k
4,7k//27k
10k//100k
1,5k//33k
12k//18k

Fig. 3.9.2

blanked signals into the required polarity. YAS, R-Y and B-Y are combined in a resistor matrix of W, R, G, B and S. Three output amplifiers supply signals meeting standards to 75 Ohms. The colour bar amplitude corresponds to R, G, B signals, having 75 % of the amplitude of peak white as it is common today. The first half of the white level range also has 75 % amplitude and the second half 100 %. On the one hand, in the colour matrix of the receiver the matrixing of R, G, B signals may thus be checked by comparing the colour ranges with the 75 % white level, and, on the other hand, the dynamic range of amplifiers may be checked with the 100 % white level.

V-sync pulses and V-blanking were omitted as this is a measuring signal. Of course, the signal may also be reproduced on a monitor which will operate on the natural video frequency and without any line interlacing. A power supply of + 6.4 V will be sufficient. In case of 12 V systems, a dropping resistor and a simple stabilizer are incorporated.

Technical data:

V_{X1}	Operating voltage	+ 12 V
$\Delta V_{X1}/V_{X2}$	Operating voltage tolerance	± 10 %
I_{X1}	Power consumption	max. 350 mA[3])
V_{X25}	(B-Y)-output	1.335 V_{pp}[1])
V_{X27}	(R-Y)-output	1.05 V_{pp}[1])
V_{X29}	(YAS) output	1.4 V_{pp}[1])
$R_{X25, 27, 29}$	Internal resistance	75 Ω
f_H	Line frequency	15625 Hz
$\Delta f_H/f_H$	Tolerance	< 1 %
t_S	Sync pulse duration	6.4 µs
t_{HB}	Horizontal blanking time	12.8 µs
t_R	Rise time	max. 30 ns
t_F	Fall time	max. 30 ns
t_C	Colour bar width	6.4 µs
t_{W75}	White bar duration 75 %	3.2 µs

[1]) at 75 ohms
[3]) V_{X1} = 13 V

t_{W100}	White bar duration 100 %	3.2 µs
t_O	Black bar duration	6.4 µs
a_C	Relative colour bar amplitude	75 %[2])

Colour sequence:	black	
	blue	
	red	
	purple	
	green	75 %
	cyan	
	yellow	
	white	
	white	100 %

3.10 Grid and white level generator (FB 45-02)

Different test signals are required for development and service of TV sets. The device shown in **Fig. 3.10** supplies all signals necessary for static and dynamic tests of the deflection, raster correction and convergence circuits. Geometry and raster pairing may be checked with a grid, the static and dynamic picture stability with a white field or white bar. All test signals may be superimposed separately or combined via a NAM-mixer (non additive mixing). The signal which in each case is set to the highest instantaneous value, will appear at the output. In this way the grid may always be used as a reference. The signal generator operates independently and all signals are produced digitally.

A crystal-controlled multivibrator oscillating at a 20-times the line frequency (312.5 kHz) serves as a clock generator. The line frequency is produced in a divider chain (FLJ 121, FLJ 161). The H-components for blanking, sync pulses, white bar and white field are produced in a decoder (FLH 281). Needle pulses for the vertical grid lines are produced by the differentiation of the 312.5 kHz pulses.

The lines are counted for the vertical division. The CCIR standard requires a 24:1 divider (FLJ 121, FLJ 171) and the FCC standard a 20:1 divider (FLJ 121, FLJ 161). The output of this divider chain is connected to a 13:1 divider. The picture frequency is generated at

[2]) converted to R, G, B signals, referred to 100% for peak white

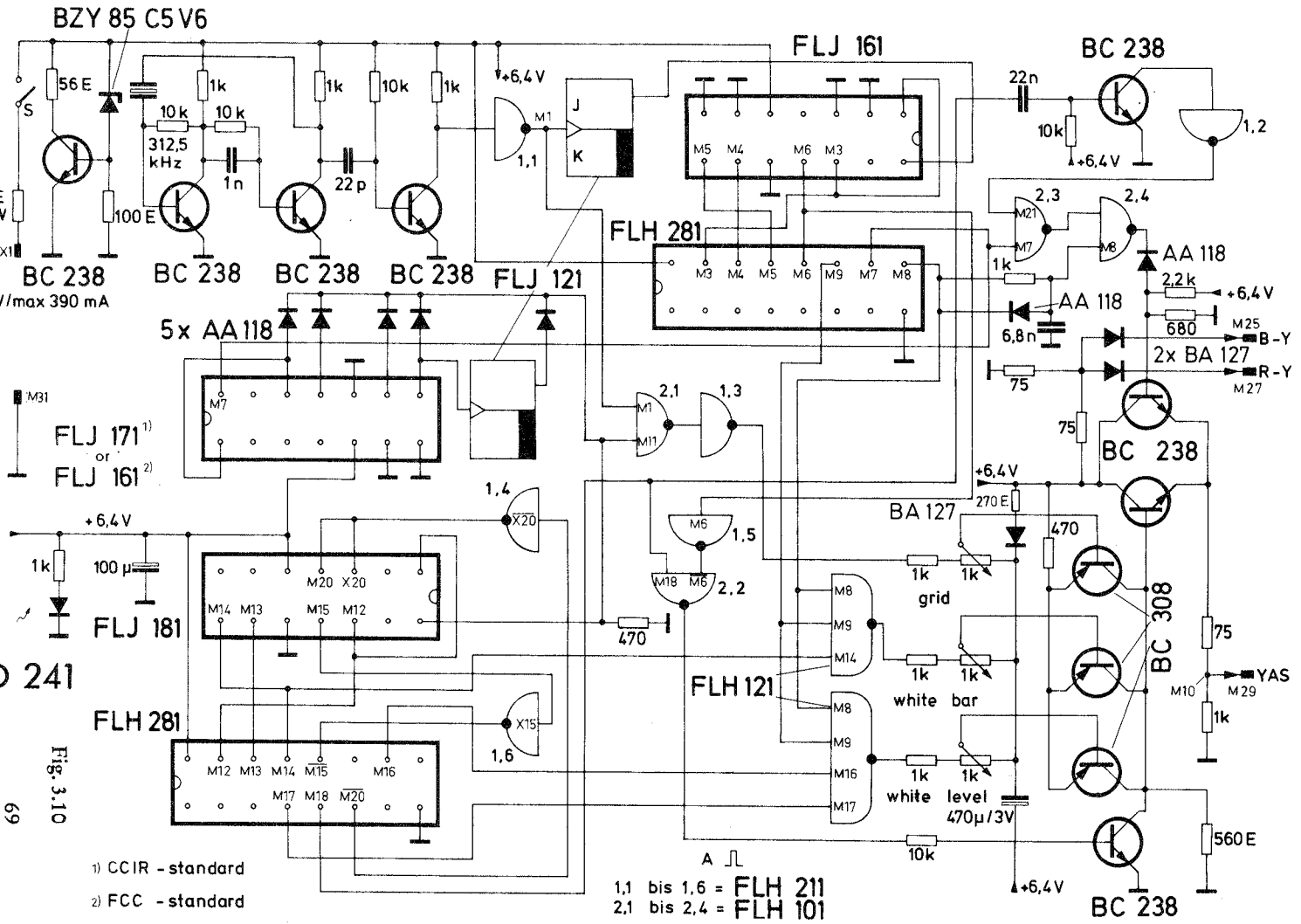

BZY 85 C5 V6
56 E
S
15 E 2 W
X1
BC 238
+12 V/max 390 mA
100 E
10 k
312,5 kHz
10 k
1n
1k
22 p
1k
10k
1k
BC 238
BC 238
BC 238
+6,4 V
M1
1,1
J
K
FLJ 121
5x AA 118
M7
M31
FLJ 171 1)
or
FLJ 161 2)
+6,4 V
1k
100 µ
FLJ 181
LD 241
FLH 281
M20 X20
M14 M13 M15 M12
M12 M13 M14 M15 M16
M17 M18 M20
X20
X15
1,4
1,6
470
M6
1,5
M18 M6
2,2
2,1
1,3
M1
M11
FLJ 161
M5 M4 M6 M3
FLH 281
M3 M4 M5 M6 M9 M7 M8
FLH 121
M8
M9
M14
M16
M17
1k grid
1k white bar
1k white level
470µ/3V
10k
A
1,1 bis 1,6 = FLH 211
2,1 bis 2,4 = FLH 101
1) CCIR - standard
2) FCC - standard
BC 238
22n
10k
+6,4 V
1,2
2,3
2,4
M21
M7
M8
AA 118
1k
AA 118
2,2k
+6,4 V
6,8n
680
M25
B-Y
2x BA 127
R-Y
M27
75
75
BC 238
+6,4 V
270 E
BA 127
470
BC 308
75
YAS
M10
M29
1k
560 E
BC 238

Fig. 3.10

the output of this divider. The generator operates without any line interlacing. For the CCIR standards we obtain 312 lines per picture (instead of 312.5) and for the FCC standards 260 lines (instead of 262.5). The picture frequency is 50.08 Hz and 60.1 Hz, respectively, referred to a line frequency of 15625 Hz. If a 314.685 kHz crystal (line frequency 15734.25 Hz) is used for the FCC standard the frame frequency is 60.52 Hz.

Another decoder LFH 281 is used to generate the V-components for blanking, synchronization, white bar and white field. The horizontal grid lines are produced via a diode gate. The grid has 12 × 16 fields. 1 vertical field and 4 horizontal fields correspond to the blanking time. The white field has 10 × 14 fields, the white bar 4 × 14 fields. As line interlacing is not used the V-sync pulse is simplified, lasting 2.5 lines. However, it is synchronous to the line and divided. The signal components are combined with the aid of gates (FLH 211, FLH 101). The NAM-mixer incorporates 3 transistors BC 308. Blanking is done with a BC 238 and S-superimposition with 2 BC 238.

A power supply of + 6.4 V is sufficient, however, a dropping resistor and a simple stabilizer are provided for 12 V systems.

Besides the YAS output there are two further outputs which are connected to a DC voltage of + 3 V via 2 switching diodes (R-Y, B-Y). The device may thus be connected with other test signal generators to a common signal bus containing three signal lines (YAS, R-Y, B-Y). The signals of a certain block are selected by switching diodes) of the tive operating voltage. The output stages (or switching diodes) of the other circuits are reversed through the signal of the selected block.

If R, G, B signals are to be used instead of (R-Y, B-Y), (YAS) signals, the three outputs in the grid generator are connected to the emitter of the output stage via 75-ohm resistors.

Technical data:

V_{X1}	Operating voltage	12 V
$\Delta V_{X1}/V_{X1}$	Operating voltage tolerance	± 10 %
I_{X1}	Current consumption	max. 390 mA[3])
V_{X25}	(B-Y)-output	+ 1.5 V[1])
V_{X27}	(R-Y)-output	+ 1.5 V[1])
V_{X29}	(YAS)-output	1.4 V_{pp}[1])
$R_{X25, 27, 29}$	Internal resistance	75 Ω

f_H	Line frequency	15625 Hz
$\Delta f_H/f_H$	Line frequency tolerance	10^{-4}
Z_{CCIR}	Number of lines CCIR	312
Z_{FCC}	Number of lines FCC	260
n	Number of fields per picture	1
f_{VCCIR}	Picture frequency CCIR	50.08 Hz
f_{VFCC}	Picture frequency FCC	60.10 Hz
t_S	Sync pulse duration	4.8 µs
t_{V1}	V-pulse 1	56 µs
t_{V2}	V-pulse 2	28 µs
t_R	Rise time	max. 30 ns
t_F	Fall time	max. 30 ns
t_{GV}	Vertical grid lines	max. 100 ns[2])
t_{GH}	Horizontal grid lines	1 line
X_H	Number of horizontal fields	16
X_V	Number of vertical fields	12
t_{HB}	Horizontal blanking time	12 µs
t_{VBCCIR}	Vertical blanking time CCIR	1.248 ms = 19.5 lines
t_{VBFCC}	Vertical blanking time FCC	1.04 ms = 16.25 lines

[1]) at 75 ohms
[2]) bandwidth at 50 % down
[3]) V_{X1} = 13 V

4. Control and regulating circuits

4.1 Temperature control circuit for boilers with proportional differential control (NO-7219)

There are varying heating-up rates in boilers operating on proportional controls, depending upon load. In summer, with a closed mixing valve and no heat requirements for the radiators, it amounts to 23 °C/min, for instance, which leads to a thermal overshoot from 90 °C to 110 °C. When operating with a working mixer, switched-on circulating pump and load by the radiators, heating-up rates of approx. 3 °C/min will occur. In this case, the overshoots may be neglected.

A temperature control circuit (Fig. 4.1) has been devised limiting the water temperature to a set point independently of the heating-up speed. An operational amplifier operating as a differentiator supplies an output voltage which depends on the heating-up speed. This voltage is fed to the non-inverting input of the switching amplifier via a transistor.

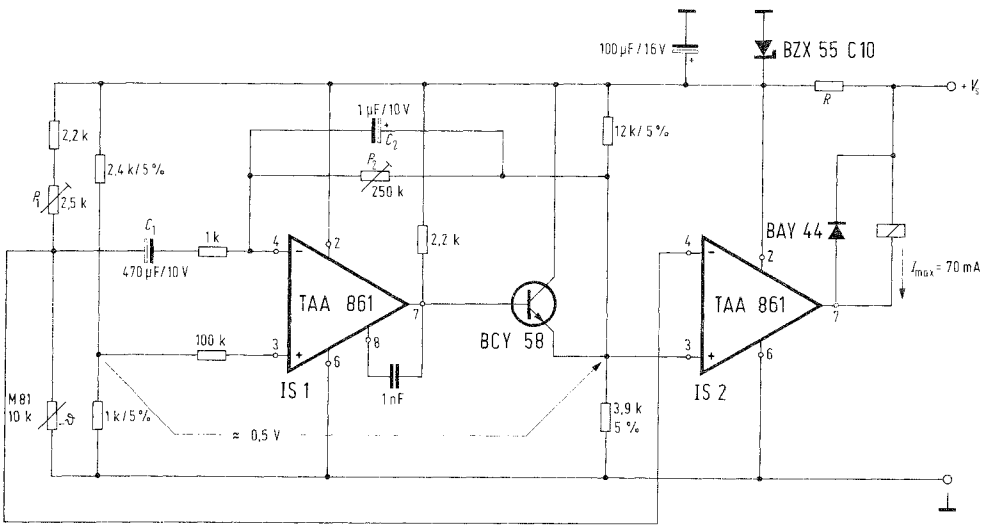


Fig. 4.1

The thermistor voltage is applied to the inverting input. The higher the heating-up speed, the earlier an interruption of the heating process.

A practical test revealed an overshoot of 2 °C (nominal temperature 90 °C) in all cases of load.

The measuring thermistor M 81/10 kΩ is arranged in a bridge circuit. The boiler temperature may be set by means of potentiometer P_1. The thermistor tolerances at nominal temperature are thus equally balanced. The thermistor voltage now lies across the inverting input of the switching amplifier as a real value, the bridge voltage across the input of the differentiator. The bridge voltage variation with time is differentiated and available at the output as a voltage. The differentiating section consists of the capacitor C_1 and the trimming potentiometer P_2, which may be used to aligne the capacitance tolerance and to adjust the differential portion of the control to the entire heating system. The potential is held at the non-inverting input of the switching amplifier by the voltage divider. With rising temperature, the output voltage of the differentiator increases, the transistor drives and raises the potential at the non-inverting input. This entails a reduction of the switching temperature of the relay. The sharper the temperature change, the lower the switching temperature. A negative differential voltage in case of a temperature reduction has no influence because of the transistor. Fluctuations around the nominal temperature will diminish with an increase of the time constant $T = C_1 \times P_2$ of the differentiator. The relay switching point corresponding to temperature also decreases.

The operating voltage is fixed in accordance with the relay at a maximum relay current of 70 mA.

4.2 Switching amplifier for solenoid valve with BDY 88 (NP-7240)

The switching amplifier using BDY 88 (Fig. 4.2) operates without a pre-stage and withstands short-term short-circuits. The switching amplifier may be driven by LSL circuits.

The resistance to short-circuits is achieved by the transistor BCY 58 limiting the short-circuit output current to the nominal current of the valve.

The circuit dimensions were chosen with respect to a solenoid valve $R = 56\ \Omega$, $L = 50$ mH.

When the emitter resistor R_E is matched, solenoid valves with switching currents up to 1 A at 24 V may be operated. As the short-circuit

power dissipation is $P_{VK} \approx 0.55\ V/R_{E2} \times V_B$ the emitter resistor should have an optimum value.
The permissible short-circuit time is determined by the size of the heat sink and the short-circuit power dissipation.

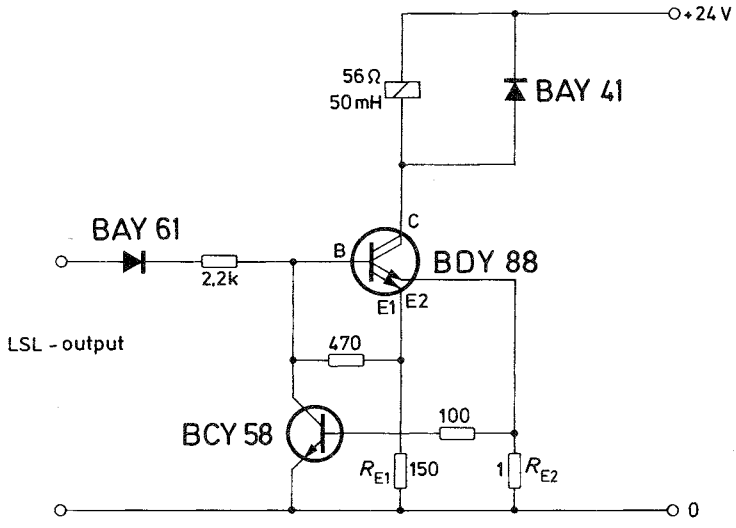
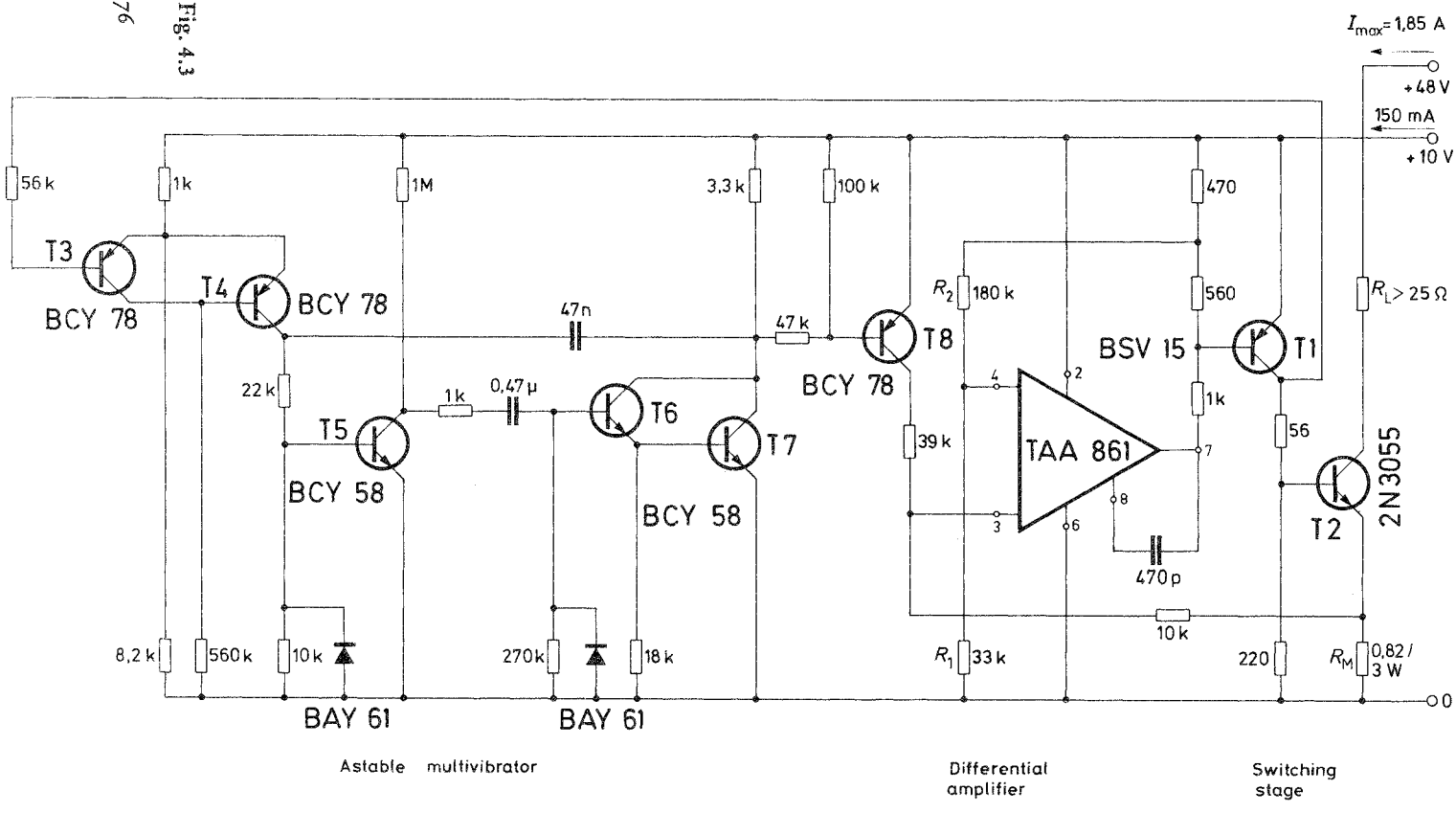


Fig. 4.2

4.3 Fuse with automatic turn-on (NP-7202)

The presented electronic current control circuit turns off at a 1.5-fold nominal current, i. e. at 1.85 A, and turns on automatically after a short-circuit has been cleared or a sufficiently large load resistance is given. The circuit (**Fig. 4.3**) consists of a differential amplifier TAA 861, a switching stage T_1 and T_2 and an astable multivibrator T_5, T_6 and T_7 with the trigger transistors T_3 and T_4 and the decoupler T_8. The current which is limited by the load produces a voltage drop at resistor R_M, which is compared with the voltage of the divider R_1/R_2 at the input of the op amp TAA 861. The voltage is set by R_1 and R_2 to 1.52 V. With a lower voltage drop across R_M the op amp remains switched

Fig. 4.3


I_{max}= 1,85 A
+48 V
150 mA
+10 V
56 k
1k
1M
3,3 k
100 k
470
T3
BCY 78
T4
BCY 78
47n
47 k
R_2
180 k
560
R_L> 25 Ω
T8
BCY 78
BSV 15
T1
22 k
1k
0,47 µ
T6
T5
BCY 58
T7
BCY 58
39 k
TAA 861
1k
56
2N3055
T2
470 p
10 k
8,2 k
560 k
10 k
270k
18 k
R_1
33 k
220
R_M
0,82 / 3 W
0
BAY 61
BAY 61
Astable multivibrator
Differential amplifier
Switching stage

through, as well as the switching transistors T_1 and T_2. The astable multivibrator and the decoupling stage T_8 are reversed by the triggering stages T_3 and T_4.
When the load reaches too low an ohmic value the op amp limits the output current. The voltage across the collector of T_1 rises, T_3 switches through and thus reverses T_4. The astable multivibrator is released. T_8 switches through after a short interval and raises the potential across the non-inverting input of the op amp. Thus the switching transistor T_2 is completely blocked. During the pulse interval of the multivibrator T_8 is reversed, the op amp switches and T_2 turns on. When the ohmic load is still too low the op amp throws back again and the operation described is repeated. After the overload has been removed T_3 becomes conducting during the pulse interval, the multivibrator blocks and the load current may flow freely.
The load control is performed at a high mark-to-space ratio (40:1) so that even in case of a short-circuit the integrated power dissipation at the switching transistor remains very small.

Technical data:

Operating voltage	10 V ± 5 %
Current consumption	150 mA
Load circuit voltage	48 V
Max. ambient temperature	60 °C
Release current	1.85 A
Pulse interval	500 ms
Pulse duration	12 ms
Heat sink	25 K/W

4.4 Delay circuit with TAA 865 (NM-7312)

It is relatively easy to achieve long delay-times with the operational amplifiers TAA 861/865/A. When the operating voltage V_S is applied to the delay circuit in **Fig. 4.4** the relay connected to the output of the op amp picks up immediately. It drops out again, however, after the preset delay time has passed.
A corresponding magnet or signal lamp could also be used instead of the relay. The function of the circuit is given by the fact that, during the starting moment, the resistor divider voltage V_T lies across the inverting input (—) while the non-inverting input (+) is more negative because of the as yet uncharged capacitor C_1.

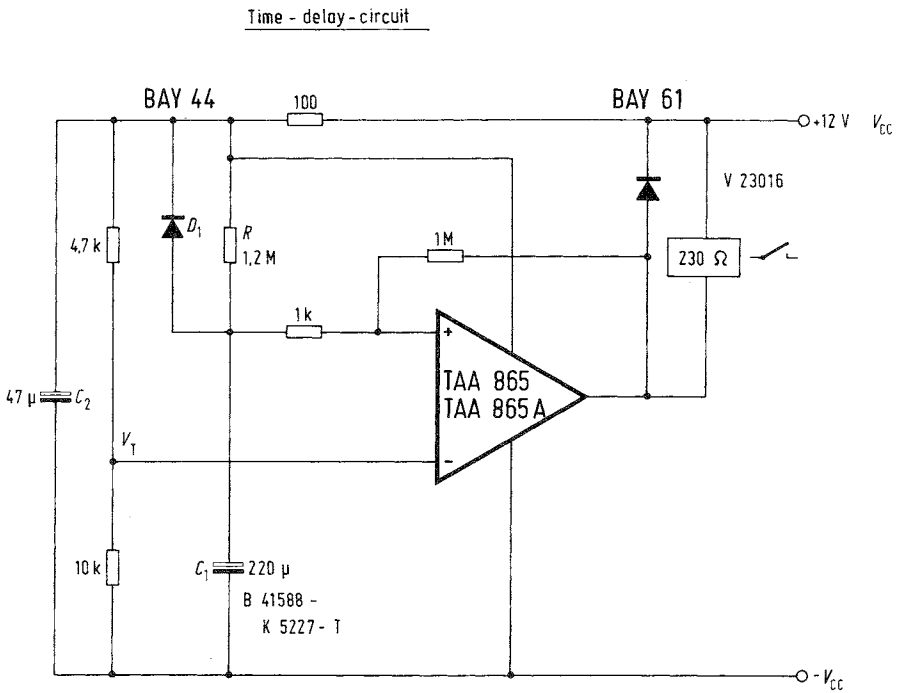


Fig. 4.4

The op amp is thus conducting and the relais has picked up. This condition, however, will prevail only until the voltage of the capacitor C charged via resistor R has reached the value V_T across the divider. The non-inverting input is then more positive and the output of the amplifier is reversed. The resistors 1 kΩ and 1 MΩ serve to generate a defined switching threshold.

The divider voltage was chosen in a way that the delay time will precisely correspond th the time constant of the RC_1-section. The delay time may thus be calculated in accordance with the following equation:

$$t_v\,[\mathrm{s}] = R\,[\Omega] \times C\,[\mathrm{F}]$$

Because of the high leakage currents in case of electrolytic capacitors, the capacitor should not reach a higher value than 1000 µf. The resistor R may be varied between 1 kΩ and 1.2 MΩ.
The diode D_1 provides for a short repetition time. It bridges the resistor R during the voltageless state and rapidly discharges the capacitor via the low-ohmic divider resistors.

Technical data:

Operating voltage V_S	12 V ± 20 %
Delay time t_d	approx. 260 s
Repetition time t_{rep}	approx. 12 s
Relay	V 230 16 A — 0005 — A 101
Switching power	120 W = 3.5 kW ~

4.5 Three-phase current phase-angle control for star and delta circuits (with 100 triacs) (NP-7231)

A triac control circuit has been developed especially for ohmic loads in a way that 100 loads operate in parallel with a nominal power of 3 kW maximum each. They may be operated in star or delta connection on three-phase networks with 130, 220 or 380 V. The power is controlled by the phase angle.
The control amplifier compares the set and the real value and feeds a voltage corresponding to the control deviation to the phase angle control circuit which is required for each phase. The temperature nominal value is set by means of potentiometer P. The true value is supplied, for instance, by a thermistor. For manual control operation, the nominal frequency selector may be directly connected to the phase-angle control.
A delta connection of the loads is only feasible if the triacs are incorporated in the phase line. Therefore a potential separation is required between the triggering and control circuits. The potential-free signal transmission from the phase-angle control circuit to the triac triggering circuit is performed with the new optoelectronic coupler CNY 17. Up to 100 triacs (3 kW max. each) may be simultaneously triggered by the three power stages.
Anti-interference sections are required in the load circuit of the triacs.
The op amp IS 1 (**Fig. 4.5.1**) amplifies the differential signal between the set and real value and supplies an output voltage of about 0 to +6 V. A following integrator R_1, C_1 is used to avoid hunting. The

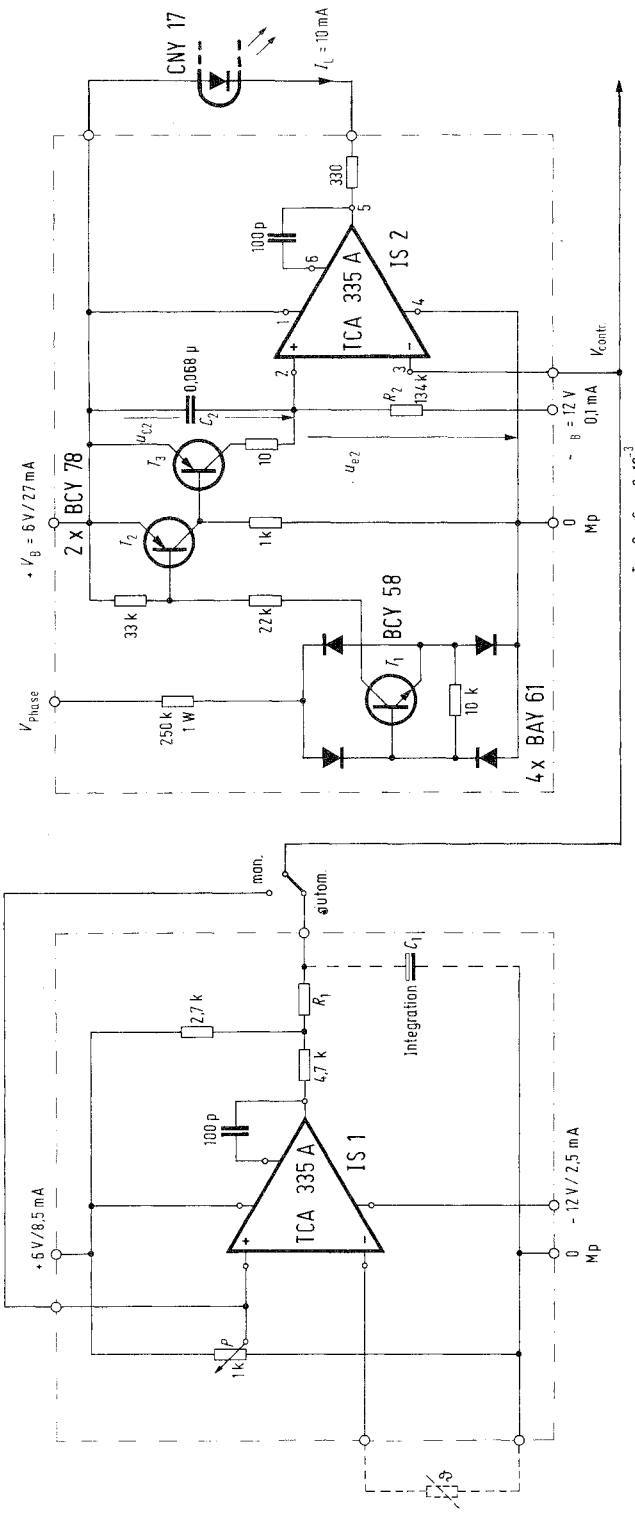

control amplifier
Phase - angle control circuit
+ 6 V/8,5 mA
0 Mp
- 12 V/2,5 mA
TCA 335 A
IS 1
100 p
2,7 k
4,7 k
1 k
P
mon.
autom.
Integration
C_1
R_1
CNY 17
I_L = 10 mA
330
100 p
TCA 335 A
IS 2
0,068 µ
C_2
R_2
134 k
$V_{contr.}$
- V_B = 12 V
0,1 mA
$I_2 = R_2 \cdot C_2 = 9 \cdot 10^{-3}$ s
+ V_B = 6 V / 27 mA
2 x BCY 78
T_3
T_2
10
1k
33 k
22 k
u_{e2}
u_{c2}
V_{phase}
250 k 1 W
T_1 BCY 58
10 k
4 x BAY 61

Fig. 4.5.1

nominal frequency selector, potentiometer P, is connected to the stabilized voltage $+ V_B = 6$ V.
Op amp I_{S2} feeds current to the light-emitting diode of the optocoupler CNY 17, when the voltage $u_{E2} = + V_B - u_{C2}$ drops below the control voltage.
The capacitor C_2 is charged via resistor R_2. The time constant $T_2 = R_2 \times C_2$ was selected in a way that during a half-cycle of the 50 Hz AC voltage (t = 10 ms) the voltage u_{C2} falls from + 6 V to 0.
The triggering circuit 4.5.2 consists of a power output stage with 2 × 2 N 3055 and of a threshold switch with BSV 15 and BCY 58. It is triggered by the optocoupler (CNY 17).

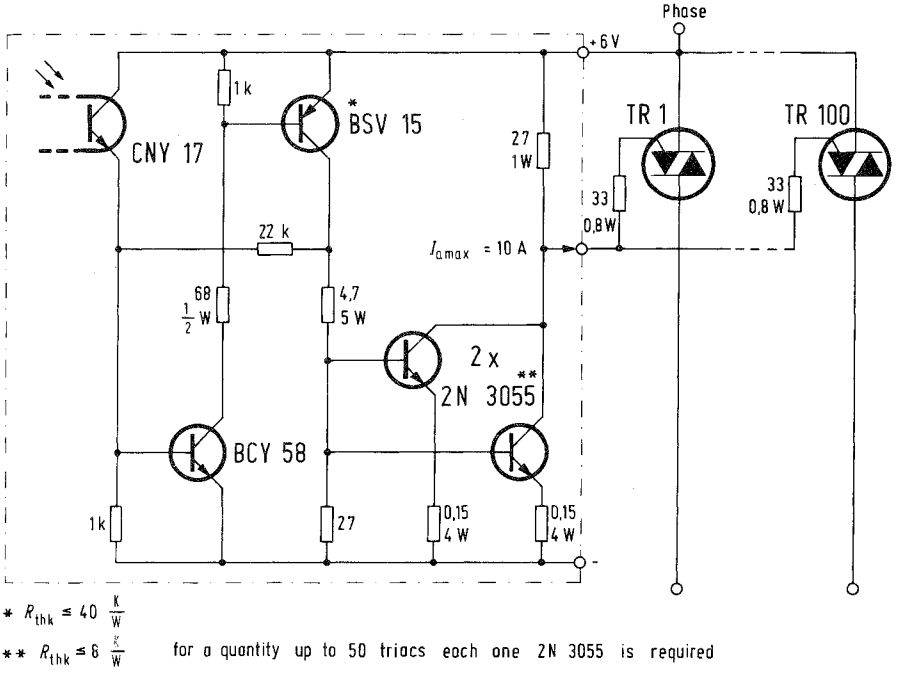


Fig. 4.5.2

The power output stage may fire up to 100 triacs simultaneously. The power supply of the triggering circuit has not to be stabilized.

Selection of triacs.
The following triacs are suggested for different loads:

Nominal voltage (50 Hz)	Max. nominal power	Nominal current	Triac	S_v*)
130 V	0.5 kW	4 A	TX C01 A40	2.18
220 V	1 kW	5 A	TX C01 A50	1.61
380 V	2 kW	5 A	TX E99 A90	1.67
380 V	3 kW	8 A	TX E99 A90	1.67

*) Selected voltage safety factor

5. Circuits with optoelectronic and magnetic devices

5.1 Transducers for DC and AC currents (NG-72083 a)

The transducer shown in **Fig. 5.1** may be used for a no-voltage measurement of DC currents with changing polarity or of AC currents.

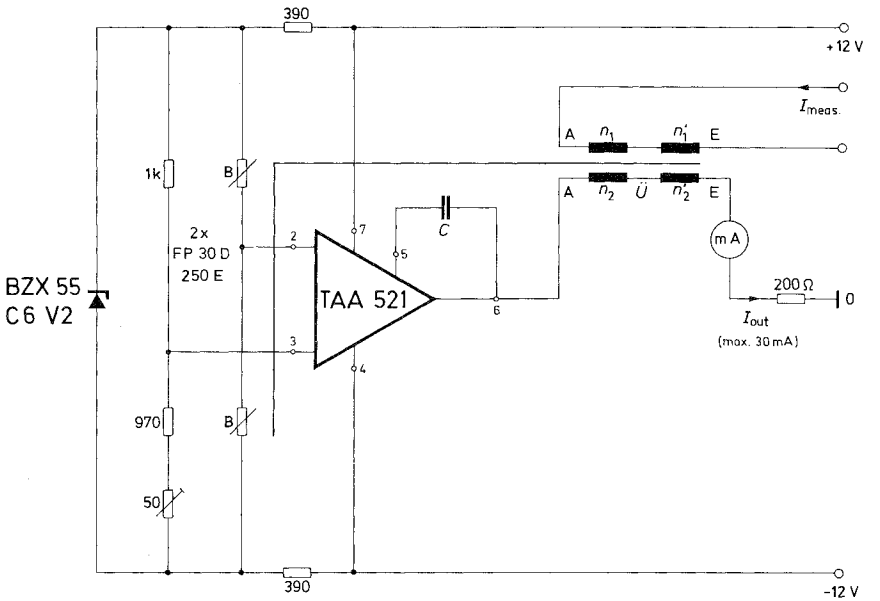


Fig. 5.1

Two magnetoresistors arranged in a magnetic circuit operate as measuring sensors. Design of the magnetic circuit, arrangement and dimensions of windings are described in "Design Examples of Semiconductor Circuits" 1973, Chapter 5.6.

Positive and negative output currents may be generated at low losses by the push-pull output of the op amp TAA 521.

Op amp TAA 521 controls the output current in a way that the magnetic induction produced by the measuring current is compensated and that the ampere-turn values of the two coils are identical.
The amperemeter indicates the output current. The total load resistance of the op amp should be $> 200\ \Omega$.

5.2 Light-barrier with LD 261/BPX 81 (ELE-720714)

Fig. 5.2 shows an light-barrier for scanning of punched cards. It essentially consists of the light-emitting diode LD 261 and a photo transistor BPX 81 with a following amplifier transistor BCY 58. When light strikes the photo transistor the latter and the following transistor will switch through. A current of approximately 8 mA is generated and a voltage drop of $V_0 \approx 3.2$ V occurs at resistor R_3. Under darkened conditions, a current of about 1 mA flows. The maximum light/dark current ratio therefore is appr. 1 : 8.

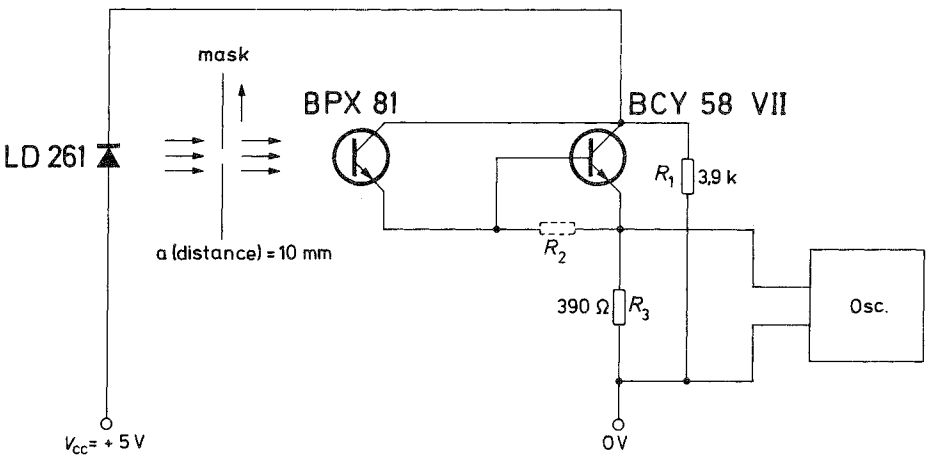


Fig. 5.2

When $R_2 = \infty$, the response limit is already reached with standard punched cards also outside the holes. With this resistor, a sensitivity correction (or setting) may be obtained for the switch-off point.

The switch-on limit (no absorption in light path = switching to high current) is reached with a resistor R_2 of approx. 300 kΩ.

In this design, the load on the light-emitting diode LD 261 is, on an average, considerably lower than in conventional designs where the diode draws current continuously.

This arrangement switches when the amplification through the feedback circuit exceeds the value of 1 (electrically and optically). The ambient light therefore does not lead to any switching operation, however, it may overdrive the circuit. With an optically unshielded design, an ambient light of approximately 200 lx is permissible in practice.

The switching hysteresis amounts to approximately 25 % referred to the switching point light/dark.

When a TTL circuit is connected a reverse current will flow via resistor R_3 in the switched-off state so that there will be a voltage drop of up to 0.63 V across R_3. The input voltage must be $\leq$ 0.8 V for the TTL circuit to recognize the state as being 0. In case of possible deviations of dimensions, this resistor may be changed and chosen $\geq$ 100 Ω at $V_B = 5$ V.

5.3 Circuit for extremely low illuminances (ELE-720615)

Automatic exposure meters (**Fig. 5.3**) are described in which the photo current of an optoelectronic sensor is integrated over the exposure time. Photo resistors do no longer operate satisfactorily in case of low illuminances, neither do commercial photo diodes. The special photo diode BPX 63 therefore was developed to mark a particularly low reverse current. In the known circuits, the signal voltage is directly amplified; in this case an inverse feedback which changes with time provides that only the signal voltage variation is utilized during the exposure period.

The aim is to control exposures even at illuminances of 10^{-2} lx fully automatically. But even the signal voltage of 0.5 mV available with the new diode is still too low for a direct DC voltage amplification.

A novel circuit (**Fig. 5.3**) for automatic exposure meters has therefore been developed. The light permanently strikes the photo diode D_1. When the switches S_1 and S_2 are closed the photo current is short-

circuited. The field effect transistors T_1 and T_2, together with the resistors R_1 and R_2, operate as source follow-ups. The gate current

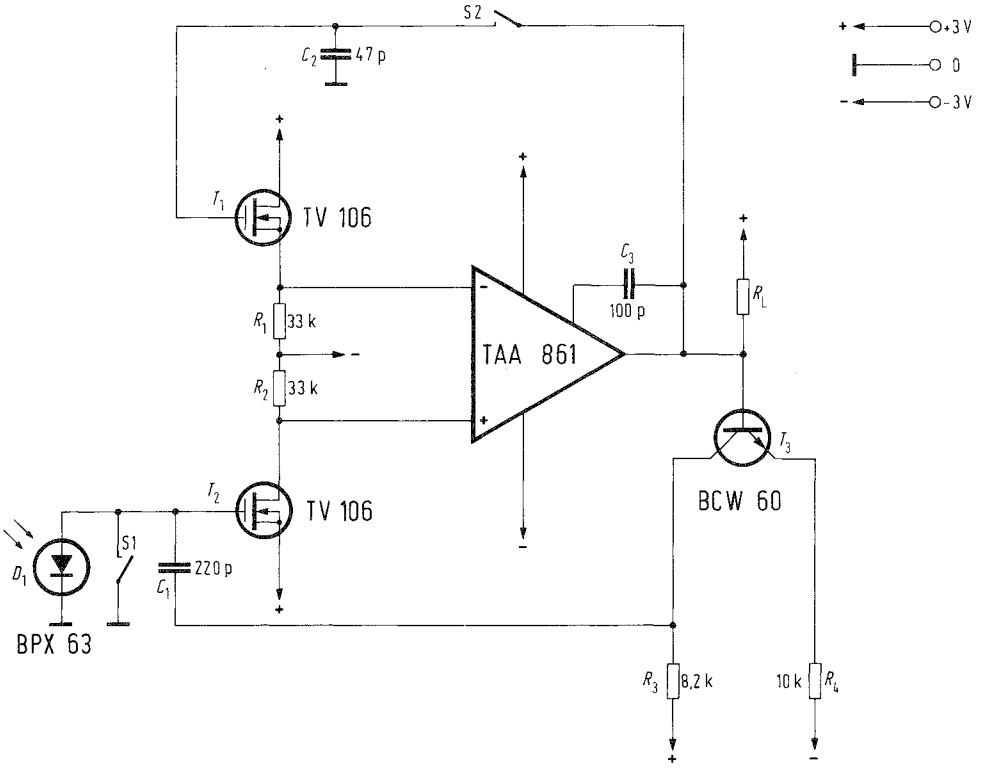


Fig. 5.3

of the FET T_1 must be considerably lower than 1 pA because the circuit cannot differentiate between photo current and gate current. When the switch S_2 is closed the output of the op amp is connected with its inverting input via the FET T_1. The transmission coefficient of the inverse feedback path thus formed is almost 1. The voltage trans-

mission coefficient from the control electrode of each field effect transistor to the op amp output therefore is also only 1. This means, however, that the drift voltage and the offset voltage of the two field effect transistors and of the op amp proceed unamplified to the output.

When the switch S_1 and also S_2 are opened the high inverse feedback is interrupted. The operating point of the FET T_2 shall not shift when S_2 is opened. The capacitor C_2 therefore stores the voltage that has been applied to the gate of field effect transistor T_1 shortly before opening the switch.

The diode photo current charges the integration capacitor C_1. The voltage across this capacitor rises linearly with time. The bipolar transistor T_3, together with the resistors R_3 and R_4, at this time only serves as a phase inverter for the output stage of the amp. This amplified and phase reversed signal lies at the base of the integration capacitor C_1. The capacitance is thus apparently increased by the loop gain — that is about 3000-fold. Relatively small integration capacitances may therefore be used. The output voltage of the amplifier was about zero at the beginning of the exposure time. During the exposure time it continuously rises to about 1 V. At this value the base voltage equals the collector voltage of transistor T_3. Now the transistor T_3 no longer operates as an amplifier. The output signal of the op amp proceeds directly, i. e. without any phase reversal — to the base of the integration capacitor C_1 via the base-collector diode path. This, however, means a positive feedback. This positive feedback has the result that the output voltage of the op amp will jump to the value of the positive operating voltage within a few microseconds. The current flowing through the load resistor R_L becomes zero. The load resistor R_L, for instance, is a traction magnet which may cause an exposure at zero current. It will do to switch on the operating voltage shortly before opening the switches S_1, S_2. The transient period that passes before we may start with the exposure time after application of the voltage is shorter than 1 ms. The capacitor C_3 is used to avoid any self-oscillation.

Shortly before switching, the output voltage of the op amp is 1 V. The difference of the source voltage drift between the two field effect transistors may not exceed 0.5 mV during the exposure. Almost any MOS FET may be used for this task provided the gate current is much lower than 1 pA. In case of lower requirements, bipolar transis-

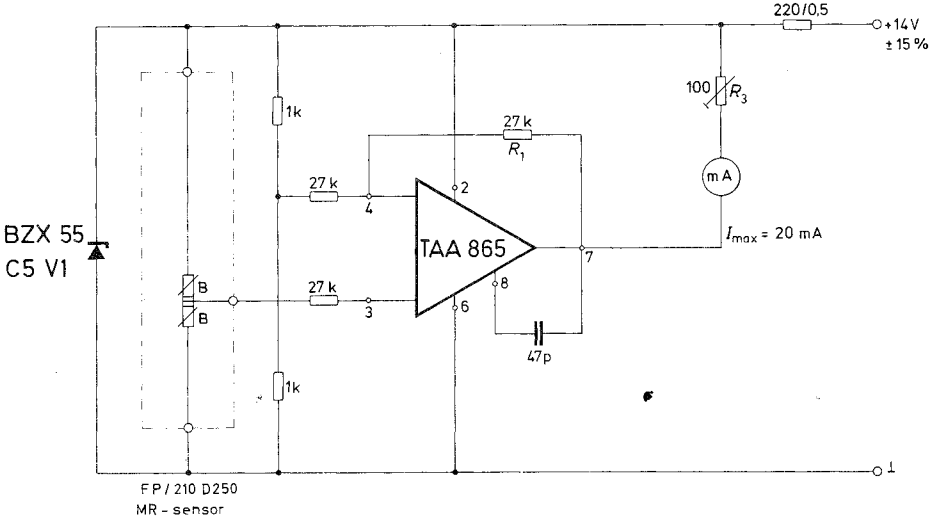
tors may also be used. The measurements were carried out with the aid of the SIEMENS experimental model TV 106.

Technical data:

Operating voltage	± 3 V
Illuminance	
(in front of filter BG 38/1.5 mm)	10^{-2} lx
Exposure time at 10^{-2} lx	12 s
Measuring error at 10^{-2} lx	< ± 20 %
Temperature range	— 30 to + 50 °C

5.4 Pressure gauge with MR-sensor FP 210-D 250 (NG-7237)

A pressure measuring circuit has been designed (**Fig. 5.4**) with the magnetoresistor pair FP 210-D250. The MR-sensor and two additional resistors are connected to a bridge, which lies at the input of op



amp TAA 865. Due to the application of an MR pair the high temperature coefficient of a single magnetoresistor in case of ambient temperature variations largely remains ineffective. The bridge voltage is stabilized by a Z-diode and is thus independent of the battery voltage, for instance. In accordance with the stroke the output current may be influencend by the feedback resistor R_1 and by the space between a small additional iron sheet and the sensor. The maximum needle deflection to both sides may be set symmetrically on center by the resistor R_2.

Technical data:

Operating voltage	14 V ± 15 %
Max. current	20 mA
Ambient temperature	— 25 to + 80 °C

5.5 AC current transmission with optoelectronic coupler CNY 17 NF-7302-09)

Optoelectronic couplers may be used not only for a floating transmission of binary signals, they also permit a potentialfree transmission of analogue signals without a transformer.

The frequency bandwidth of the coupler surpasses the requirements of AF-transmission engineering. The upper cutoff frequency is approximately 140 kHz, the lower cutoff frequency is 0 Hz. In contrast to the transformer, the coupler also lends itself to the transmission of DC currents. The non-linear distortions produced by the coupler are below 1 % provided a proper choice of circuit and operating point is made. Optoelectronic couplers may be employed in AF coupling fields and mixer units in order to avoid hum pickup, for a potentialfree connection of an AF-amplifier to a TV set, in measuring and control engineering.

Fig. 5.51 shows the transmission characteristic of a typical optoelectronic coupler, type CNY 17, with a collector resistance and a transmission coefficient of approximately 100 % at various operating voltages.

The couplers are classified in groups in accordance with the transmission ratio. The spread of each group covers ± 33 %.

In case of a high supply voltage for the sensor and a small collector resistance the inevitable tolerances take the least effect on the signal transmission.

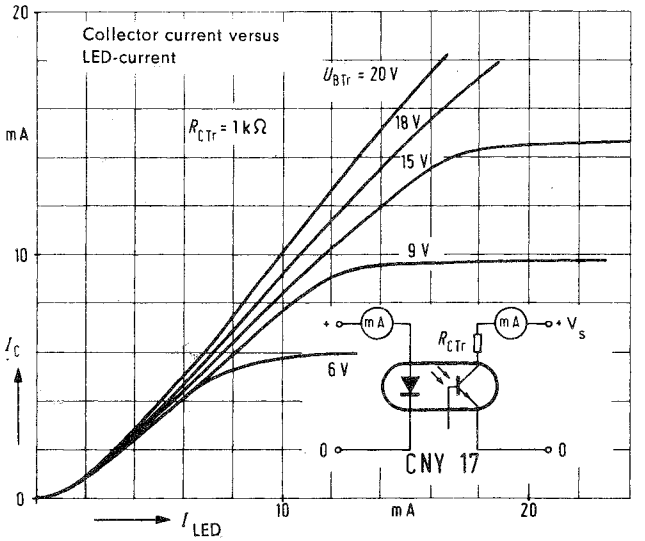


Fig. 5.5.1

The coupler, however, produces the lowest distortion factor when operated at the turning point of the characteristic. A signal transmission which is particularly low in distortions therefore requires the optimum setting of the operating point of the photo transistor. This is best done on the transmitter side of the coupler by changing the current of the light-emitting diode. Any balancing of the collector resistance may unfavourably influence the voltage-frequency-response and the dynamic characteristics.

For instance, at I_F = 5 mA, the output signal should be 80 mV for an unweighted signal-to-noise ratio of 50 db, as required for Hi-Fi engineering.

The upper cutoff frequency of the light emitter may practically not be raised by measures of circuitry. A large signal-to-noise ratio is achieved with a high input signal. Small input signals may be amplified through the emitting circuit.

Fig. 5.52 shows a basic emitting circuit. The operating point of the photo diode is set with the resistor R. For a low distortion factor, the current is controlled via resistor R_v which is considerably higher than the dynamic resistance of the light-emitting diode of approximately 10 Ω.

A high input resistance of $R_e \approx 140\ k\Omega$ and a voltage gain of $g_v \approx 16$ are shown by the circuit in **Fig. 5.3.3.**

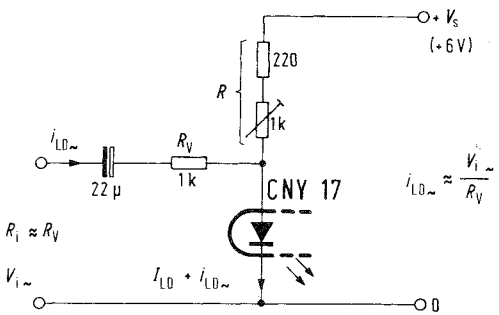


Fig. 5.5.2

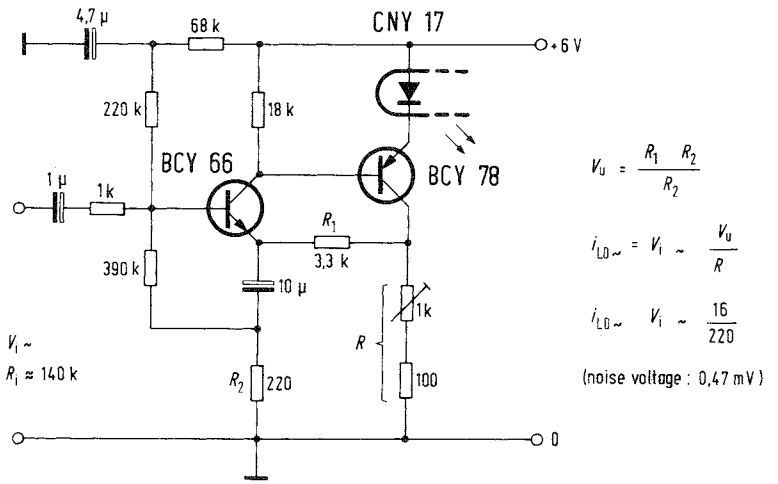


Fig. 5.5.3

The following circuit (**Fig. 5.5.4**) is suitable for transmission of higher frequencies. The upper cutoff frequency of almost 100 kHz is achieved with an AC feedback from collector to base of the photo transistor. The dynamic characteristics and the transmission ratio, however, are reduced. The signal-to-noise ratio reaches 65 db.

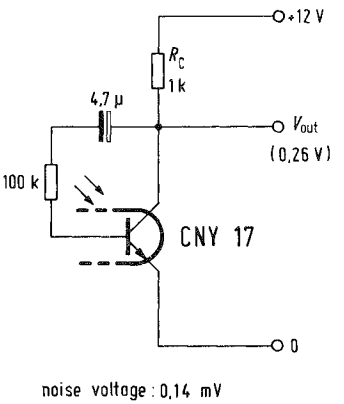


Fig. 5.5.4

A two-stage amplifier with an inverse feedback to the base of the photo transistor results in an upper frequency limit of 140 kHz, a small output resistance of 70 Ω and a great dynamic range.

5.6 Mains operation of light-emitting diodes 110/220 V (NF-7215)

Light-emitting diodes may relatively easily be operated at 110 V or 220 V AC mains, 50/60 Hz.

An indication sufficiently flicker-free for the eye is already ensured in a half-wave operation of the diode. Circuits with an ohmic or capacitive series resistance and a thyristor phase-angle control may be used. The circuit with the lowest loss is that using a capacitive series resistance (**Fig. 5.6.1**). It requires about 0.5 W or 1 W.

The arithmetic mean of the LED-current is approximately 20 mA.

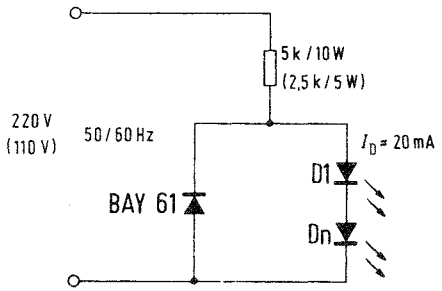


Fig. 5.6.1

The power across the series resistor is high — 10 W in case of 220 V and 5 W in case of 110 V in a circuit using an ohmic series resistor and a parallel diode (**Fig. 5.6.1**). The parallel diode only requires a reverse voltage of a few volts. It is used to keep the reverse voltage across the light-emitting diodes small during the negative half-wave.
In case of a circuit using the capacitive series impedance (**Fig. 5.6.2**) the diode current is determined by the capacitor. The resistor serves to limit the current when switched-on in the voltage maximum. A parallel diode with a lower reverse voltage will be sufficient.

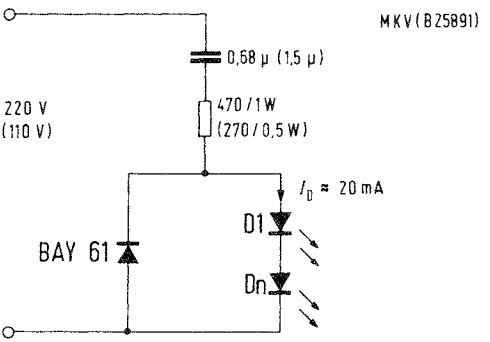


Fig. 5.6.2

For a parallel operation of several light-emitting diodes, a phase angle control as described in "Design Examples of Semiconductor Circuits" 1973, 6.2, may prove advantageously. At the end of the positive half-wave it will switch with a small angle of current flow ($\alpha \approx 25°$). The circuit may be operated without any modification with 220 V or 110 V, 50/60 Hz.

6. Power supply circuits

6.1 Sine-trapezoid switch-mode power supply 220 V ~ 2 × 40 V/1.25 A with mains separation (PN-7212-06)

Power supplies with higher frequencies enjoy considerable advantages over conventional 50 Hz power supplies, especially when a stabilized output voltage is required.

Features of the switch-mode power supply:

Mains separation (VDE) — low weight — effective balancing of mains voltage variations (± 10 % → ± 1 %) — good stability of output voltage (< 5 %) in case of load variations (— 50 %) — low hum voltage (< 1 %) — ideal switching characteristics of the switching transistor — low edge steepness (sine/trapezoid) — short-circuit proof — good alterning load characteristics — switches off in case of excess mains voltage — high efficiency (approximate 70 %) — low overall expenses.

Description of circuit:

The rectified mains voltage — the operating voltage V_B for the switching transistor T_1 — is generated across capacitor C_5 (**Fig. 6.1**) by diode D_2. The transformer Tr (L) and C_3 result in a resonant circuit with an oscillating frequency of approx. 20 kHz, which supplies the feedback voltage for the base via winding n_4. The negative feedback half-wave is kept small by the diode D_3 so that the transistor T_1 receives only about half the peak-to-peak voltage of n_4 as a reverse voltage across the base. The winding n_3 supplies, after rectification, the operating voltage for the control transistor T_2 which is controlled by the reference diode D_5.

The exact output voltage is set at R_8. The control current via T_2 causes a varying base bias across C_7 with the base of T_1 receiving more or less strong positive half-wave currents. The switching time and the collector peak current I_C are thus controlled. The secondary winding n_2 of Tr forms the output part together with D_1, C_2, Dr 1 and C_1, which supplies the rectified and filtered output power of 2 × 40 V/ 1.25 A.

The oscillating frequency depends on the load and the operating voltage. The curve shape changes from a sinusoidal to a trapezoidal shape. The oscillator circuit L—C_3, in conjunction with the biased base control, is used to obtain an "ideal" switching behaviour. The base

control only sets in when the collector oscillating voltage has reached the value of zero. In the following charging phase of the transformer inductance L the collector current I_C rises from negative (inverse) values continuously up to a defined (by the control part) peak current. The switch-off phase of the current causes the collector current to fall towards zero before the collector voltage across the switching transistor may rise. The capacitor C_3 wants to maintain its voltage while the current I_C has sufficient time to fall off.

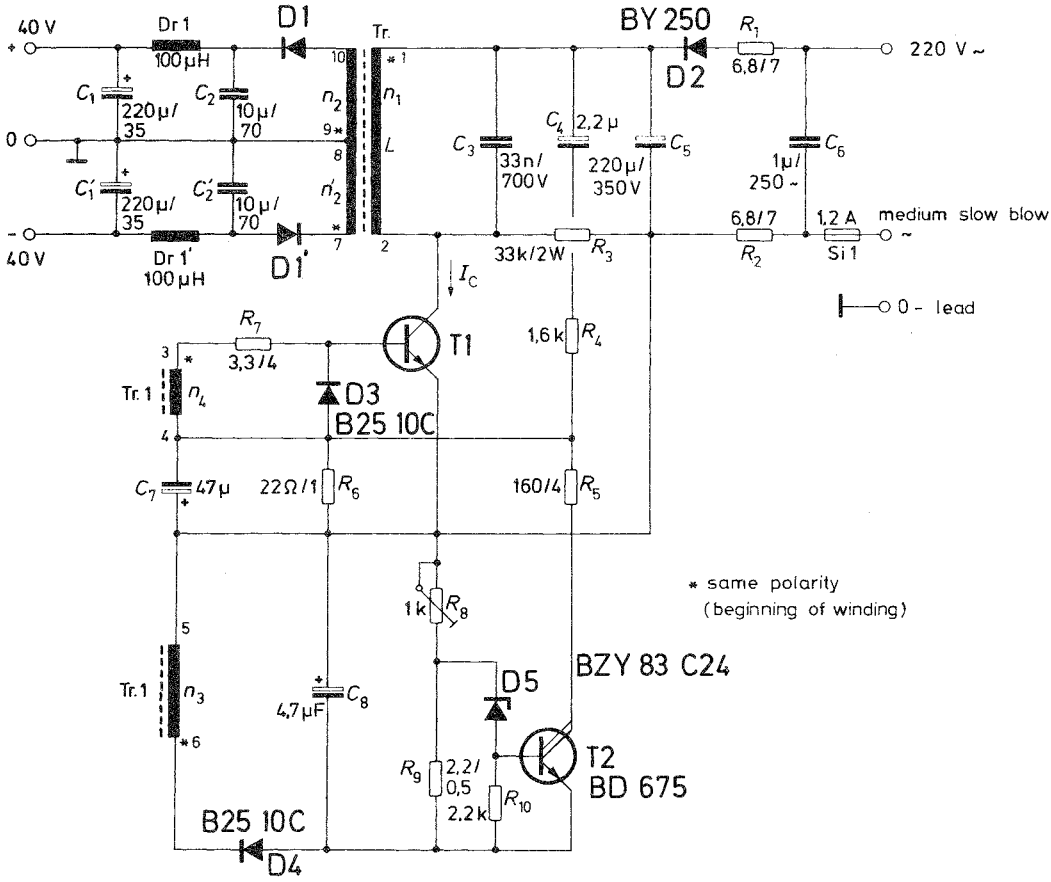


Fig. 6.1

With more or less DC bias across the base more or less fedback base AC voltage is controlled, with the switch-on time of the transistor becoming longer or shorter. Single or two-stage DC current amplifiers may be used as variable gain amplifiers (T_2). Two-stage amplifiers produce an improved stabilization of the output voltage at lower hum voltage, however, with an unfavourable RF filtering in the amplifier, they more easily tend to AF hunting. With the darlington amplifier here provided for hum values of $\approx 1\,\%$ ($V_{pp\,h}$) are achieved with nominal load. The mains voltage (220 V_{rms}) is rectified by means of a half-wave rectifier.

Under low load, the DC voltage rises from 0 V to approx. 200 V within 3 to 4 ms, and after 20 ms further to 260 V within 3 ms and again after 20 ms to 290 V within another 2.5 ms. After about 5 × 20 ms the final state is achieved. Under load, the voltage rises somewhat more slowly and reaches its balanced condition at, for instance, 260 V. It may therefore be concluded that during the first rise in voltage the RF oscillation must set in early enough so that the switching transistor, from the very beginning, starts to oscillate under very good (ideal) switching conditions. If oscillation would only set in at higher voltages, impermissible losses may occur in the family of characteristics.

Switching characteristics

The circuit has been designed in a way that the active family of characteristics is not covered above all in the range of higher sensitivity against overload. There are virtually only the states "current" or "voltage" with the transistor. This ideal switching behaviour becomes feasible only with an oscillating circuit in conjunction with the delayed control provided for in this case. This oscillator circuit principle offers a further advantage, namely that the transformer for mains separation may be realized much more easily because square-wave voltages do not have to be transmitted.

Switch-on behaviour

In case of large secondary charging capacitors (C_2!) the initial load is higher and lasts for a longer period of time. The transformed overall value of the secondary charging capacitor may not be dimensioned too large.

After switching on, the oscillation at first starts with about 5 oscillations of a lower frequency ($^1/_3$ to $^1/_2$ f) and has reached the nominal frequency at about 15 to 20 oscillations. With the capacitor C_5 completely discharged, the oscillation fires approximately at $V_B = 100$ V. The buildup time constant of the oscillating system should be smaller than the switch-on time constant of the rectified mains voltage because the oscillation buildup will thus always remain within the permissible range of characteristics. A relatively rapid rise of the RF-AC voltage against the rising operating DC voltage shall thereforce be warranted. In any case, it must be ensured that the oscillations switch through completely. The resistors R_1 and R_2 on the mains resp. C_5 must therefore dimensioned large enough.

Decay behaviour and rapid reswitching

Within the family of characteristics the decay takes such a course that the operating loop becomes continuously smaller until the oscillation is broken off at approximately $V_B = 50$ V. The circuit may be switched on again immediately and without any danger. The oscillation is "fired" then a little later than with a completely discharged capacitor C_5.

Switch-off behaviour in case of load short-circuit

The kickback supplies energy to the charging capacitor C_2 via the high-speed diode D_1. In case of a short-circuit, after the rise of the voltage across C_3 from $V_{CE} = 0$ a sufficient voltage can by no means be generated as of V_B, which would permit an oscillation from $V_{C\,max}$ down to $V_{EC} = 0$ (only $\pm V$ referred to V_B is feasible). The base AC voltage thus remains much too small to get from the reverse voltage across capacitor C_7 into the positive control zone $V_{BE} \geqq 0.6$ V. The transistor T_1 remains reversed immediately and safely. The oscillation stops. The voltage across C_7 is reduced considerably more slowly than the circuit voltage which, strongly damped by the short-circuit, decays.

Switch-off behaviour in case of excess mains voltage

With a rise in mains voltage the charging time of the transformer inductance L via the transistor becomes shorter. Under constant load, however, the discharging time via diode D_1 must remain constant because an equal amount of energy is taken away. The control circuit, however, forces shorter transformer charging times by the transistor, and the voltage amplitude of the negative half-wave ($= V_B$) rises.
The voltage of the positive half-wave, however, only permits an influence to such a maximum negative value which corresponds to the

preceeding positive half-wave, i.e. with a further increase in V_B the flyback voltage, $V_{CE} = 0$, is no longer achieved. Thus there is also no more "firing" feedback voltage. The voltage across capacitor C_7 reverses the transistor and the oscillation breaks off damped with R_3. Connection of the power supply to an impermissibly high excess voltage will lead to its immediate switching off after a short build-up. The power supply is thus also excess-voltage proof.

Alternating load behaviour, electric strength of switching transistor

An alternating load from 100 % up to about 1/10 of the nominal load is feasible and permissible. When the filtering capacitors C and C_1 are not large enough, however, a short-term unloading as well as loading in the excess voltage range may cause the oscillation to switch off. The transformer may not be dimensioned too small, i.e. the positive oscillating voltage should be chosen at least 10 % higher than the maximum "charging oscillating voltage". The latter should equal the maximum rectified excess mains voltage. We thus arrive at a maximum collector-emitter voltage for the transistor of $V_{CE\,max} \geqq 1.1\ V_{B\,max} + V_{B\,max} = 2.1\ V_{B\,max}$*). A switching transistor with $V_{CEV} = 750$ V for an excess mains voltage of 250 V_{rms} will just do for alternating load operation from $N_{o\,nom} \rightarrow N_o = 0$. With constant load the demands on the collector voltage V_{CEV} are reduced to approximately 600 to 700 V.

Open-circuit behaviour

The power supply, on principle, permits unloading up to the open-circuit state. With a break-off of oscillation, the decay time constant of the oscillating circuit L-C_3 must be smaller than the time constant of the base wiring R_6–C_7 so that there will be no "refiring" (control) during the unloaded decaying operation. With an insufficient damping (R_3) any restriking might jeopardize the transistor.

Control range, hum voltage

The simplest control amplifier is a single-stage DC current amplifier as shown in **Fig. 6.1.** The control range is larger with a lower load than with a higher load. Mains voltage variations of ± 10 % are well balanced under nominal load to approximately ± 1 % and less, especially when a mains bridge-connected rectifier is used instead of the single diode.

*) without overshoot at transformer

Switching-on again after a short-circuit or turning off an excess voltage. With a secondary short-circuit or turning off an excess voltage the operating voltage rises to its peak value and remains at this value until switched off on the mains side. The capacitor C_5 may, for instance, be discharged via the resistor R_3. This resistor also constitutes a basic damping for the oscillating circuit — which is important in case of an automatic switching-off of excess voltage. The ideal solution is to induce a very rapid discharging of the mains electrolytic capacitor with the mains switch turned off. The mains switch should then be designed as a change-over switch.

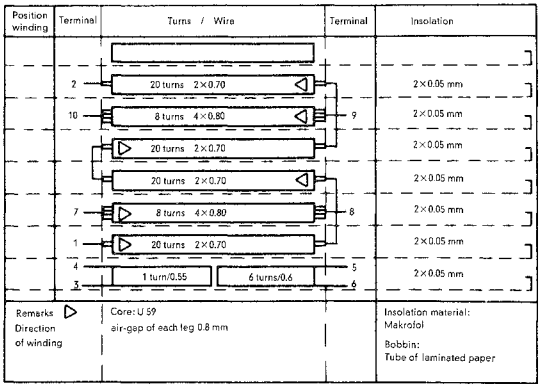
Interference behaviour

As the edges of the RF-AC voltage are by far not as steep as with square-wave voltages the capacitive spurious RF-radiation is low. The remaining magnetic radiation may be largely reduced by shielding which must be connected with the mains neutral wire (earthing contact-type plug), when a low radio interference is to be obtained. Same has to be done with the ground wire on secondary side.

Semiconductors:

T_1	transistor TV 146a (development sample)
T_2	transistor BD 675
D_1, D_1'	diode E 3010 (with heat sink 15 cm²)
D_2	diode BY 250
D_3	diode B 2510 C
D_4	diode B 2510 C
D_5	Z-diode BZY 83/C 24
Dr_1/Dr_1'	10 mm ϕ × 40 mm L $\approx$ 100 µH (with AF core)
Tr	oscillating transformer (U 59)

Transformer data:



6.2 Sine switch-mode power supply for halogen projector lamp 12 V/100 W

The design of the RF power supply circuit shown in **Fig. 6.2** for a 100 W halogen projector lamp is remarkably simple. The lamp is directly fed by the secondary winding. Besides the 50 Hz power supply it only consists of a siferrite transformer U 59 (or U 56) and the switching transistor with base RC-section and starting section $R_3 \ldots C_3$. The lamp power is adjusted with the base resistor.

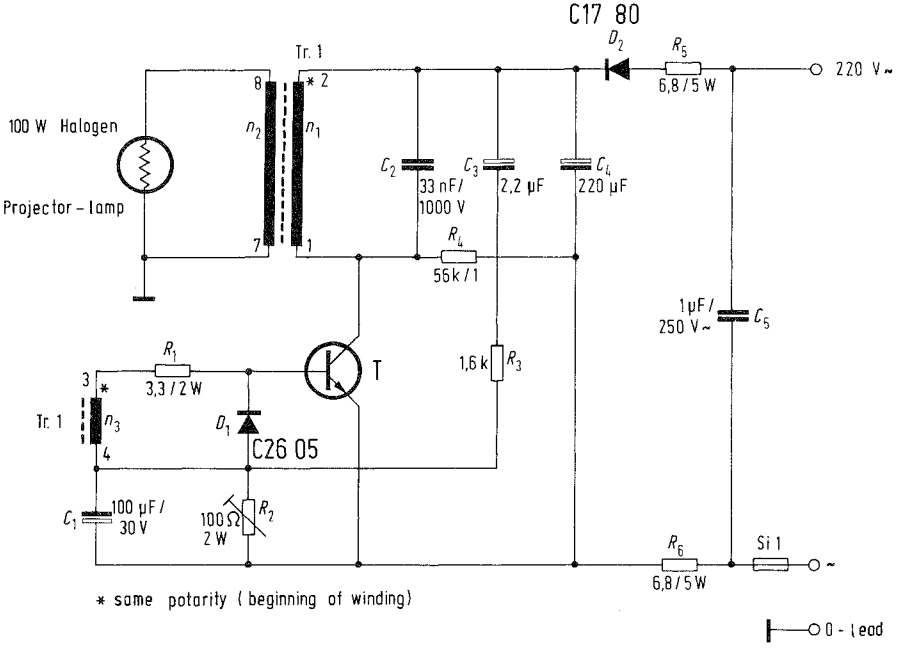


Fig. 6.2

In principle the circuit operates as described in chapter 6.1.
The secondary winding (7 . . . 8) must here be arranged on the second leg of the U core so that a certain leakage between the secondary and primary winding is achieved. This is important because the halogen lamp practically constitutes a total load short-circuit during the switching-on.

The power supply is short-circuit proof and open-circuit proof. Under no-load conditions (lamp is defective!) the collector voltage rises to approximately 1100 V so that in this case a transistor must be used reversing at higher values (BU 108). If a certain control effect shall come to bear in case of mains voltage changes a single-stage control device has to be added, as described under 6.1. This also includes the reference winding (5 . . . 6) at the transformer.

Transformer data:

Core: Siferrite U 59, material N 27
Air gap: 0.8 mm per leg
Winding

1 . . . 2	80 turns	2 × 0.7 mm ϕ CuL (leg 1)
3 . . . 4	1 turn	0.5 mm ϕ CuL (inside, leg 1)
5 . . . 6	4 turns	0.5 mm ϕ CuL (leg 1)
7 . . . 8	5 turns	6 × 0.7 mm ϕ CuL (leg 2)

6.3 Controlled DC voltage converter 24 V-5 V/5 A with current limitation (NR-7301)

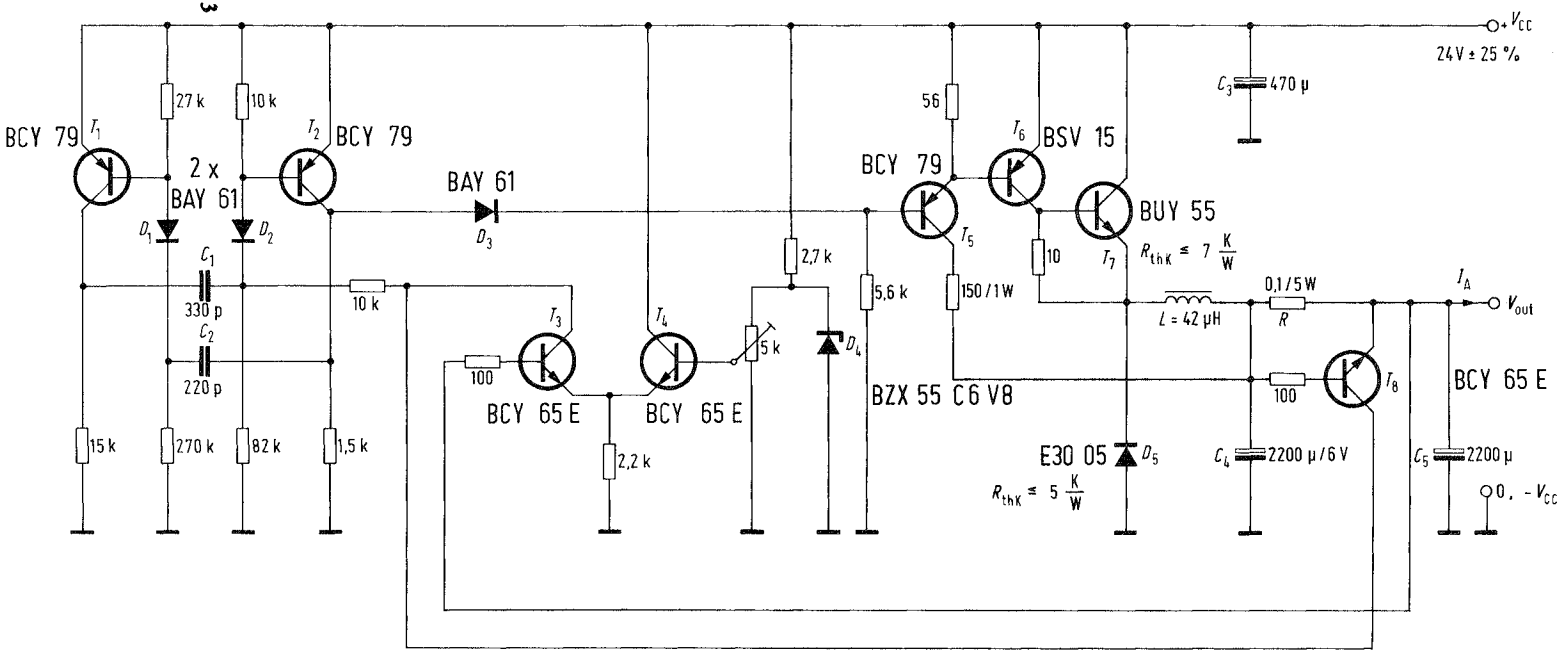
A DC voltage converter with voltage control and current limitation has been designed with the high-speed, triple-diffused power transistor BUY 55 and the high-speed power diode SSiE 3005 serving as switching stages. The control frequency of the transformer lies above the range of audibility at about 20 kHz.
The DC voltage converter permits a mains-independent emergency power supply for TTL circuits from a 24 V accumulator as required in power plants and plants with similar security demands. It is characterized by its high efficiency of about 70 %.

Technical data:

Operating voltage	24 V ± 25 %
Oscillating frequency	≈ 20 kHz
Output voltage	5 V (3 . . . 6 V)
Max. output hum voltage	20 mV_{pp}
Min. output current	0.3 A
Max. output current	5 A
Current limitation at	≈ 5.5 A
Voltage stabilization factor $\frac{\Delta V_A}{V_A} : \frac{\Delta V_B}{V_B}$	0.04
Internal resistance	17 mΩ

DC - DC - converter 24V - 5V / 5 A
(Voltage regulation , Current limitation)

Fig. 6.3



Efficiency at $V_B = 24$ V, $V_A = 5$ V

I_A	[A]	0.5	1	2	3	4	5
η	[%]	61	65	70	68	68	67

Thermal resistance of heat sink for

T_7 $\leqq 7$ K/W

D_5 $\leqq 5$ K/W

Circuit description:

The DC voltage converter consists of the astable multivibrator T_1, T_2 whose pulse interval is determined by the control transistors T_3 and T_8, and of the switching stage T_5, T_6, T_7.

The power transistor BUY 55 charges the storage inductor L and the charging capacitor C_4. When the transistor T_7 is reversed the inductor feeds energy to the capacitor C_7 and continues to charge it. The capacitor C_4 is continuously discharged via the output DC current over the entire period.

An additional filtering of the output voltage is obtained through the resistor R and the capacitor C_5.

The differential amplifier T_3, T_4 compares the output voltage with the reference voltage across the trimmer potentiometer 5 kΩ and controls the reverse time of T_2 via T_3, which approximately corresponds to the switch-on time of T_7.

The transistor T_8 serves to limit the output current. As of 5.5 A, the current will be limited. The output voltage will then fall off and the inductance may discharge itself only little. The short-circuit current therefore rises to about 7 A.

Output currents of below 0.3 A may no longer be adjusted by the multivibrator so that the output voltage rises. A basic load may possibly be required.

6.4 20 kHz thyristor power supply 220 V ~/5 V=40 A (PN-7212)

The power supply described represents a short-circuit proof and open-circuit proof 20 kHz switch-mode power supply 220 V, 5 V, 40 A, using the thyristor BSt CC 0146 R and the high-speed diodes SSi E 3005 and SSi E 3015, suitable for professional applications, such as data and communication engineering.

The self-oscillating thyristor power supply here shown is a very safe switch-mode power supply. The presented design only supplies a single

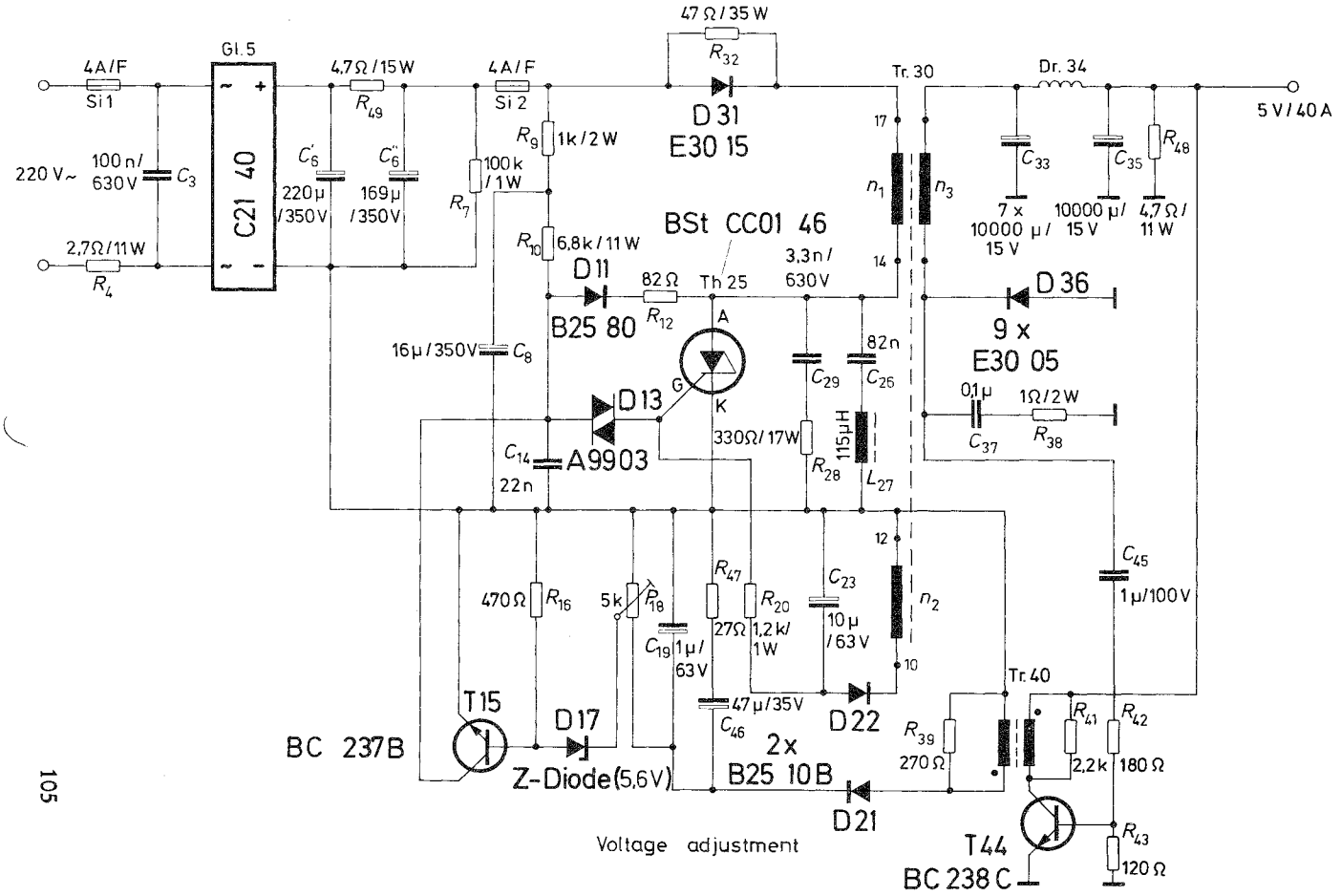

47 Ω / 35 W
R_{32}
Gl. 5
4 A / F
Si 1
4,7 Ω / 15 W
R_{49}
4 A / F
Si 2
D 31
E30 15
Tr. 30
Dr. 34
5 V / 40 A
220 V~
100 n / 630 V
C_3
C21 40
C'_6
220 µ / 350 V
C''_6
169 µ / 350 V
R_7
100 k / 1 W
R_9
1 k / 2 W
R_{10}
6,8 k / 11 W
2,7 Ω / 11 W
R_4
BSt CC01 46
D11
B25 80
82 Ω
R_{12}
Th 25
3,3 n / 630 V
16 µ / 350 V
C_8
A
G
K
D13
A9903
C_{14}
22 n
C_{29}
C_{26}
82 n
330 Ω / 17 W
R_{28}
115 µH
L_{27}
n_1
n_3
C_{33}
7 x 10000 µ / 15 V
C_{35}
10000 µ / 15 V
R_{48}
4,7 Ω / 11 W
D 36
9 x
E30 05
0,1 µ
C_{37}
1 Ω / 2 W
R_{38}
C_{45}
1 µ / 100 V
n_2
470 Ω
R_{16}
5 k
P_{18}
C_{19}
1 µ / 63 V
R_{47}
27 Ω
R_{20}
1,2 k / 1 W
C_{23}
10 µ / 63 V
47 µ / 35 V
C_{46}
D22
T15
BC 237B
D17
Z-Diode (5,6 V)
2x
B25 10B
D21
Tr. 40
R_{39}
270 Ω
R_{41}
2,2 k
R_{42}
180 Ω
T44
BC 238 C
R_{43}
120 Ω
Voltage adjustment

Fig. 6.4

operating voltage of 5 V and may replace to advantage conventional power supplies using a mains frequency transformer and a series transistor control.

The thyristor BSt CC 0146 R represents an integrated component which is used as a switch.

An approximately square-shaped voltage is generated across the transformer. Its peak value corresponds to the DC voltage across the charging capacitor C_6.

The output voltage is stabilized to about 0.2 to 0.6 % in case of mains voltage variations of ± 10 %. In this case a mains hum of about 10 mV_{pp} to 60 mV_{pp} will remain. When the load is changed from 100 % to 25 % the output voltage change will be smaller than 1 % (40 mV). The power supply is adjusted to 5 V by means of R_{18}. The thyristor and the diodes at the output must be adequately cooled; proper heat sinks must be used.

RF power supplies operate on square-wave voltages of approximate 15 to 25 kHz at amplitudes of about 550 V_{pp}, i.e. they result in a corresponding natural interference spectrum. This radio interference or interfering voltage conduction into the mains must be prevented by suitable shielding measures (perforated or full metal sheet) as well as by chokes and blocking capacitors. Cooling must be maintained.

The efficiency achieved with this device is about 65 %. The transformer technology at higher frequencies requires particular care. Multi-wire windings, parallel as well as series circuits and, in part, RF stranded wires are required. The two legs should be wound with wire in order to improve the leakage and, above all, the cooling conditions.

The output voltage which is rectified by the transistor T 44 and transformed by the small transformer Tr 40 to the primary side serves as a control variable. In comparison with the reference diode D 17 the control transistor T 15 is controlled, which will influence the thyristor's firing time via diac D 13.

Technical data:

Mains voltage	220 V ~ 50 Hz
Output	5 V/40 A
Mains control (V_{mains} ± 10 %)	0.2 % to 0.5 %
Output voltage change (with load 100 % to 50 %)	0.25 %
Hum voltage (V_{mains} ± 10 %)	0.2 % to 0.6 %

6.5 Sine power supply with high voltage generation 220 V ~ /16 kV and mains separation

The power supply for b/w TV sets suggested below operates basically like the power supply described under chapter 6.1. However, it has a bridge rectifier instead of a half-wave one and a two-stage AGC amplifier which must be designed in a way that an excessive RF interfering voltage will not affect the control circuit. A RF filtering may influence the control speed and favour hunting, especially during unloaded operation. The operation on a TV set, however, constitutes an almost constant load. To obtain a more uniform load on the power supply it is suggested to use an (ironless) class-A push-pull output stage for AF and grid control for the video signal control. The beam load and the video output stage load are thus balanced to a more uniform transformer load.

The remaining mains hum is very low with a two-stage AGC amplifier $< 0.2\ V_{pp}$. This is supported by the constant load of the reference voltage.

The power supply (**Fig. 6.5**) supplies all voltages required in a TV set. To obtain a favourable rectification of the high voltage the transformer has to be designed in a way that a duty cycle of at least about 3 : 1 is achieved. The indirectly stabilized high voltage may thus be rectified with a suitable high-tension stick. As all required voltages including the high tension are derived from the power supply, a deflecting transistor BU 110 may, for instance, be fed via a simple and inexpensive inductor. The deflector, in this case, remains free from the transformer connection to the high tension. Therefore spark-overs may not affect the deflecting transistor.

A voltage doubler may be used for the high-tension rectification instead of a high-tension stick TV 18 S at about half the number of turns (12–13). In this case, however, a small uncontrolled share of the mains voltage ($\pm$ 1.5 %) and a mains hum voltage of ($\pm$ 5 %) remains on the high tension. These values, however, are probably still within permissible bounds.

The spurious RF radiation of this power supply precisely corresponds to a conventional tube or transistor-deflection circuit using a high-voltage transformer.

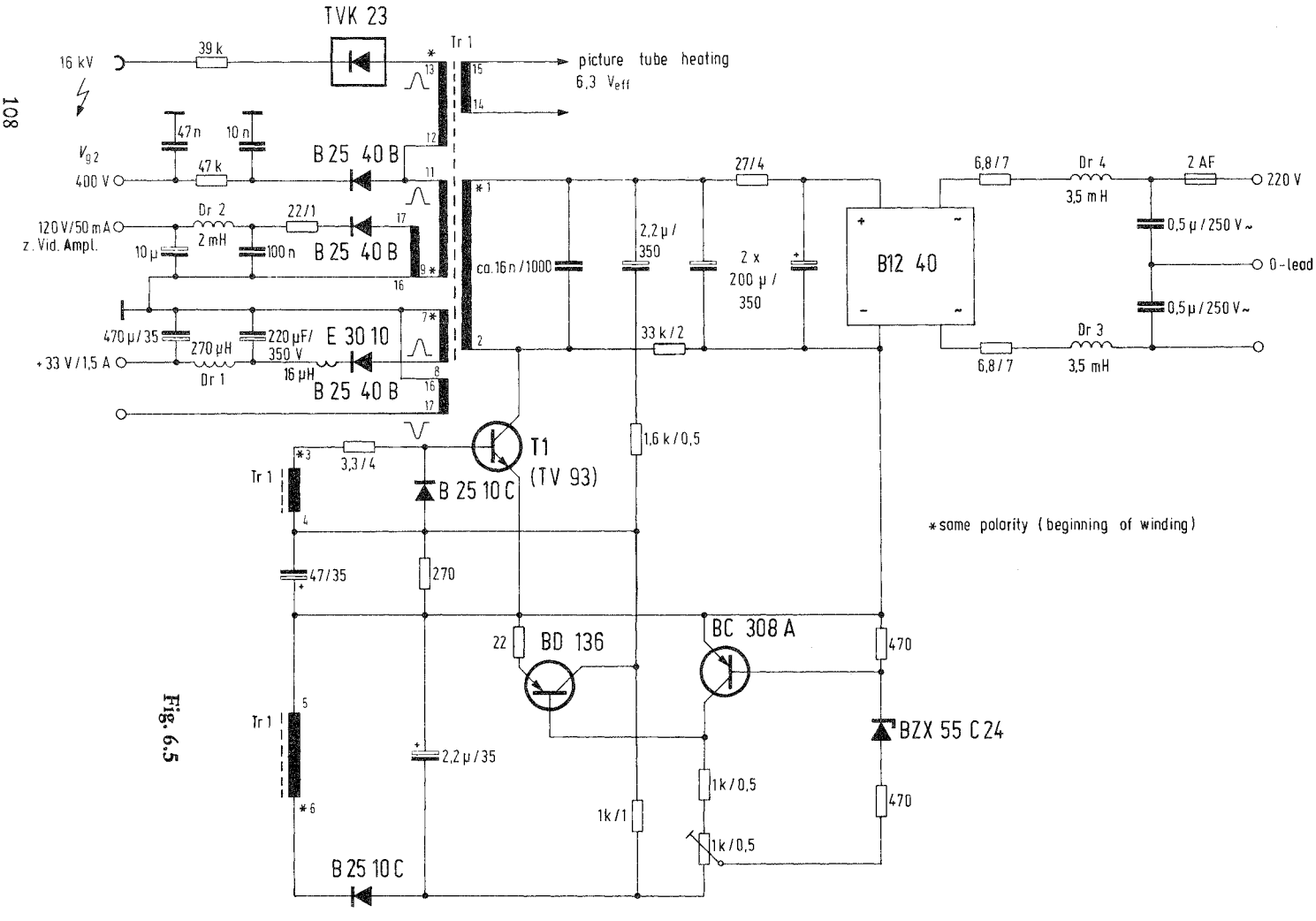

TVK 23
16 kV
39 k
Tr 1
picture tube heating
6,3 Veff
47 n
10 n
Vg2
400 V
47 k
B 25 40 B
27/4
6,8/7
Dr 4
3,5 mH
2 AF
220 V
120 V/50 mA
z. Vid. Ampl.
Dr 2
2 mH
22/1
10 µ
100 n
B 25 40 B
ca. 16 n/1000
2,2 µ/350
2 x 200 µ/350
B12 40
0,5 µ/250 V~
0-lead
0,5 µ/250 V~
470 µ/35
270 µH
220 µF/350 V
E 30 10
+33 V/1,5 A
Dr 1
16 µH
B 25 40 B
33 k/2
6,8/7
3,5 mH
Dr 3
T1
(TV 93)
1,6 k/0,5
3,3/4
B 25 10 C
Tr 1
47/35
270
22
BD 136
BC 308 A
470
BZX 55 C24
2,2 µ/35
1k/0,5
1k/1
1k/0,5
470
B 25 10 C
* same polority (beginning of winding)

Fig. 6.5

The clear advantage of this circuit, to have a separate complete power unit with mains separation, is opposed by a slight drawback, namely that the frequency is freely oscillating and any remanent RF interference must therefore be better filtered as they could influence the video range.

Transformer Tr 1

Siferrite U 57 Material N 27 L = 0.8 mm per leg

1 ... 2	141 turns 0.55 mm ϕ CuL (primary)
3 ... 4	2 turns 0.55 mm ϕ CuL (feedback)
5 ... 6	5 turns 0.55 mm ϕ CuL (reference)
7 ... 8	9 turns 5 × 0.55 mm ϕ CuL (30 V load)
9 ... 10	24 turns 0.25 mm ϕ CuL (150 V video voltage)
10 ... 11	34 turns 0.25 mm ϕ CuL (9–11, 400 V, $V_{g2} + V_{g4}$)
12 ... 13	1520 turns 0.11 mm ϕ CuL (high tension; leg 2!)
14 ... 15	3 turns 0.55 mm ϕ CuL (heating picture tube)
16 ... 17	24 turns 0.25 mm ϕ CuL (+ 150 V; leg 2, inside!)

6.6 50 Hz power supply, thyristor-controlled 220 V/175 V ± 1%

The power supply described in **Fig. 6.6** operates with a bridge of four diodes B 0540 or a bridge-connected rectifier B 1240. The 100 Hz half-wave voltage thus generated may be filtered with standard electrolytic capacitors (in this case 2 × 200 µf, B 43298 — S 4407 — 71). Control and rectification is done by a thyristor BSt B 0246 which is periodically fired in phase-angle control, which derives its firing pulses from a regulating circuit. This circuit — only a pure backward-acting regulation is being applied — consists of a voltage divider which compares part of the output voltage with the fixed voltage of a Z-diode BZY 85 C 24. The difference between these two voltages is applied as a control voltage to the base of the control amplifier transistor BC 237 B. The transistor acts as a variable resistor which influences the 100 Hz phase shifter consisting of the collector resistor (47 kΩ), the internal resistance of the transistor, the capacitor 0.1 µf at the collector and another phase-shifting RC section. The output voltage of the phase shifter is fed to the starting electrode of the thyristor via a diac (A 9903). Thus the ignition time comes after the maximum of the 100 Hz sine half-waves and is shifted on the trailing edge of these half-waves depending upon the amount of the output voltage. A standard filtering

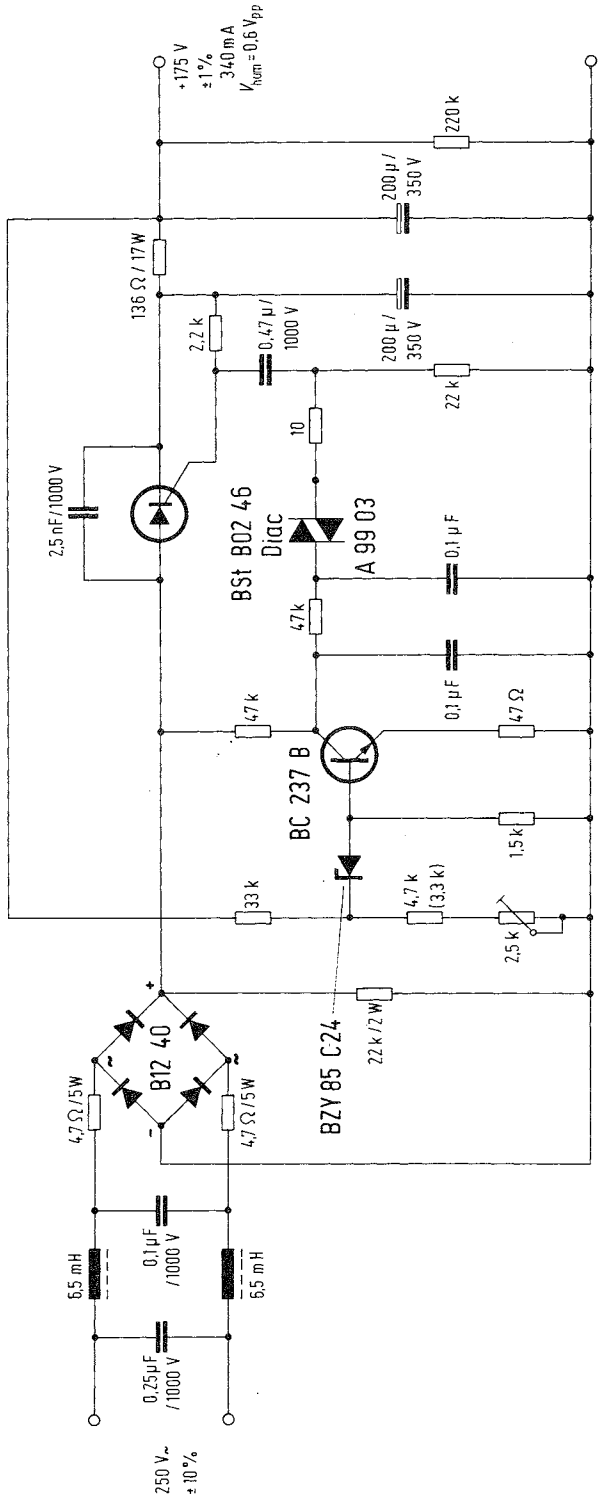

+175 V
±1%
340 mA
V_{hum} = 0,6 V_{pp}
220 k
200 µ / 350 V
136 Ω / 17 W
2,2 k
0,47 µ / 1000 V
200 µ / 350 V
22 k
10
2,5 nF / 1000 V
BSt B02 46
Diac
A 99 03
0,1 µF
47k
0,1 µF
47 Ω
4,7 k
BC 237 B
1,5 k
33 k
4,7 k (3,3 k)
2,5 k
22 k / 2 W
BZY 85 C24
B12 40
4,7 Ω / 5W
4,7 Ω / 5W
6,5 mH
0,1 µF / 1000 V
6,5 mH
0,25µF / 1000 V
250 V~ ±10 %

Fig. 6.6

section removes the superposed 100 Hz hum up to a residual of 0.6 V_{pp}. The output voltage of about 175 V is held constant to ± 1 % at ± 10 % mains voltage variations.

Data:

a) At a filter resistance of 136 Ω:
   175 V ± 1 % at 350 mA current consumption
   hum voltage: 0.6 V_{pp}
b) At a filter resistance of 100 Ω and a current consumption of 0.55 A we have an output voltage of approximately 170 V and a residual hum of 1.3 V_{pp}.

6.7 Trapezoidal power supply with mains separation 220 V/185 W (PN-7302-07)

The switch-mode power supply suggested (16 to 20 kHz) supplies an output power up to 185 W. The voltage has an about trapezoidal curve shape. The relatively small edge steepnesses (5 µsec) result in low RF interferences, which are filtered by suitable chokes and capacitors at input and output. Output voltages of, for instance, ± 24 V, + 75 V (or 2 × 75 V) and + 250 V and 6.3 V_{eff} are provided for (Fig 6.7). The mains rectification is carried out by a bridge-connected rectifier B 12 40. The electrolytic capacitors C_3 and C_4 in conjunction with the power resistor R_3 filter the pulsating DC voltage. The residual ripple is subsequently reduced to very small values by the control power supply itself. This switch-mode power supply operates in principle on the same lines as the one described under 6.1. Only the base of T_4 is triggered at a considerably higher current (approximately 1.5 A). Here, too, the oscillating circuit C_6/L_1 provides for the required time delay during the switch-on and switch-off operations. The switching transistor T_4 (Siemens development sample TV 146a or TV 148) will switch the mains DC voltage to the oscillating transformer Tr 2 at the very moment when the oscillating circuit voltage across collector T_3 has reached the value of zero.
The transistor is switched off again when the switch-off pulse arrives via the driver darlington transistor T_3 BD 675. As the switching is strongly forced at its base the switching behaviour in the family of characteristics is excellent (there are virtually only the states "current" or "voltage"!). The power dissipation remains small. The feedback voltage is generated in the winding 3 to 4. The buildup surge proceeds via C_5 and R_5 to the base of the switching transistor T_4 and raises the

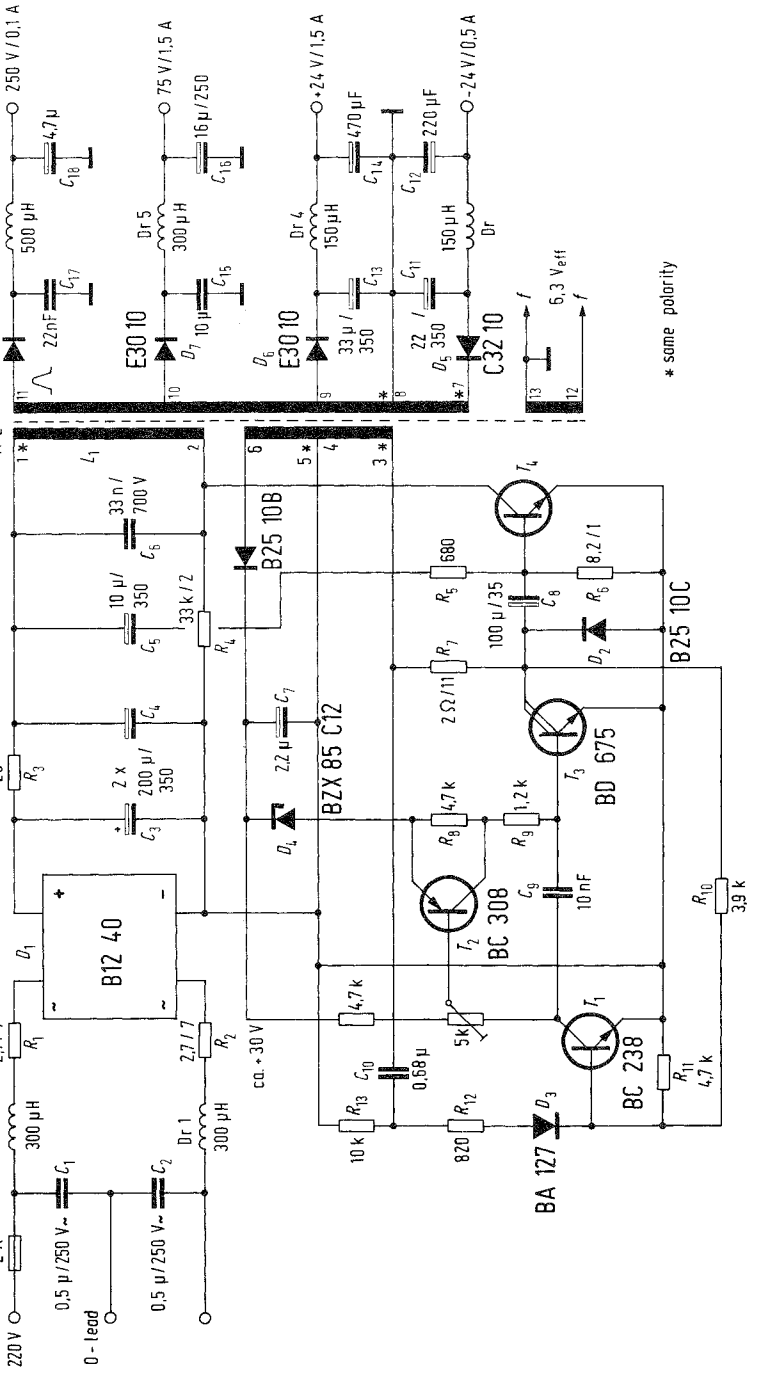

220 V
2 A
0,5 µ / 250 V~
0 - lead
0,5 µ / 250 V~
Dr 2
300 µH
Dr 1
300 µH
2,7 / 7
2,7 / 7
B12 40
20
2 x
200 µ /
350
33 k / 2
10 µ /
350
33 n /
700 V
Tr 2
B25 10B
ca. + 30 V
2,2 µ
BZX 85 C12
4,7 k
1,2 k
10 nF
5k
0,68 µ
10 k
820
BC 308
BC 238
BA 127
680
100 µ / 35
2 Ω / 11
BD 675
8,2 / 1
B25 10C
3,9 k
4,7 k
Dr 6
500 µH
22nF
4,7 µ
250 V / 0,1 A
Dr 5
300 µH
10 µ
16 µ / 250
75 V / 1,5 A
Dr 4
150 µH
33 µ /
350
470 µF
+24 V / 1,5 A
Dr
150 µH
22 /
350
220 µF
-24 V / 0,5 A
B25 80B
E30 10
E30 10
C32 10
6,3 Veff
* same polarity

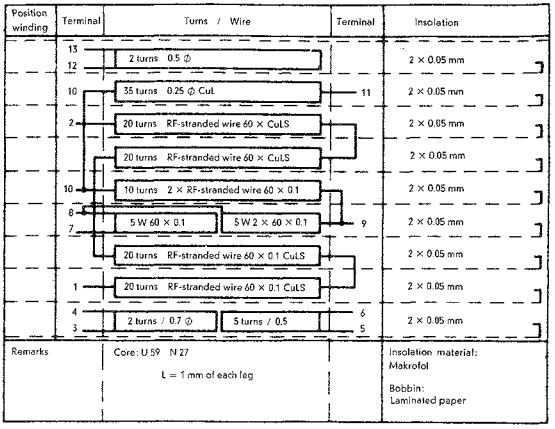
Fig. 6.7

operating point into class-A-operation for a short while whereby the oscillation is excited immediately. When the reference voltage has exceeded 12 V the Z-diode D_4 becomes conductive. At the same time the feedback voltage triggers the transistor T_1 via C_{10}/R_{12} and diode D_3. This transistor generates a pulse voltage across the collector, which is differentiated through C_9, R_8 and R_9 and controls the darlington transistor T_3 which, on its part, switches the output transistor T_4. The feedback resistor R_{10} supports the input voltage per period as long as the switching time — which is determined by the timing element C_9–R_9 and R_8 — has elapsed (monostable multivibrator). The transistor BC 308 controls the time of this timing circuit as a function of the mains and load voltage in comparison with the reference voltage across the Z-diode D_4.

The values of the secondary charging capacitors may not be too high so that the oscillation buildup will safely remain within the permissible range of the family of characteristics. Thus far the output voltage is not very rigid in case of load variation.

In case of a secondary short-circuit the oscillation will break off immediately without any postoscillation. The capacitors C_8 and C_{10} will then feed a reverse voltage to the bases of T_1 and T_4 for some time.

Transformer data (preliminary):
Core: Siferrite U 59, material N 27
Charging amplitude 3.75 V per turn
Kickback amplitude 5 V per winding



Part 2

7. Circuits using TTL-series FL 100

7.1 Power supply for TTL-circuits

Fig. 7.1 shows a power supply specially devised for TTL-circuits as its mains and load controls are mainly dimensioned for this application. The potentiometer P = 1 kΩ adjusts the required output supply voltage V_S, which is 5 V for TTL-circuits. The reference voltage necessary is generated by the Z-diode BZX 97.

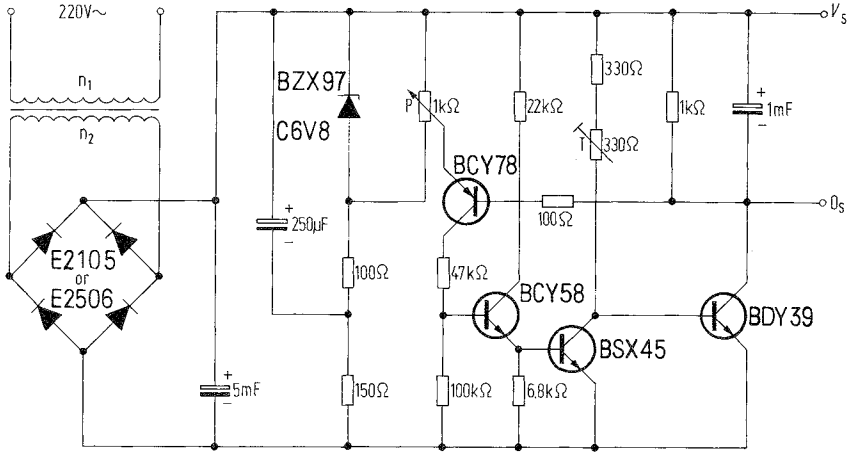


Fig. 7.1

The base of transistor BCY 78 is connected to the output, thus the stabilization of the output voltage is achieved. The transistors BCY 78, BCY 58, BSX 45 and BDY 39 form a closed control loop, whereat the output voltage is the sum of the voltage, set by the potentiometer P and the base-emitter voltage of transistor BCY 78.

The output current is max. 2 A due to the max. permissible power dissipation of the power transistor BDY 39. In order to guarantee this value for sure a resistor of 330 Ω in series with a trimmer potentiometer T is provided for. Both resistors limit the base current of BDY 39 and thus also its collector current. The max. current has to be adjusted by the trimmer potentiometer T in accordance with the current gain of this power stage.

For the operation of systems with TTL-circuits it has to be considered that additional capacitors have to be used in order to cut transients.

Technical data:

Input voltage		V_i 220 V ± 10 %, 50 Hz
Output voltage		V_S 5 V
Control range of V_S		0.7 to 7 V
Max. output current		I_S 2 A
Hum voltage		$V\sim$ < 2 mV
Control ratio at mains variations		
$\Delta V_i = \pm 22$ V;	$V_i = 220$ V;	$\frac{\Delta V_S}{V_S}$ ± 0.8 %
$V_S = 5$ V;	$I_S = 2$ A	
Control ratio at load variations		
I_S = 0 to 24 at V_i = 220 V		$\frac{\Delta V_S}{V_S}$ 2 %
V_S = 5 V		
Internal dynamic resistance		R_i ~ 50 mΩ
Ambient temperature range		T_{amb} 0 to 70 °C
Temperature coefficient of V_S		~ 0.2 $\frac{mV}{°C}$
Thermal resistance of the cooling block for BDY 39		R_{th} ≦ 2.5 °C/W
Transformer M 65 without gap, alternated layer windings		n_1 1550 turns 0.25 CuL
Dynamo sheet IV/0.35		n_2 72 turns 1.4 CuL

List of parts:

1 BCY 58, Q 60203-Y 58
1 BCY 78, Q 60203-Y 78
1 BDY 39, Q 62702-D 81
1 BSX 45, Q 60218-X 45
1 BZX 97 C6V8, Q 62702-Z 1231
1 E 2106 or E 2506, C 66067-A 1719-A 2 or Q 66067-A 1730-A 2

7.2 Binary coded counter and frequency divider

Fig. 7.2 shows a counter with variable division ratio which is binary preset in this application by the inputs A_1 to A_8. The circuits FLH 431 compare the states of the synchronous counters FLJ 431 with the preset

division ratio n. As soon as the condition $A_1 = A_{01} = B_{01} = Q_{A1}$, $A_2 = A_{11} = B_{11} = Q_{B1}$ etc. up to $A_8 = A_{32} = B_{32} = Q_{D2}$ is performed the comparator 2 supplies the reset signal at the output A = B. The reset of counters is clock controlled and occurs only at clock pulse n+1.

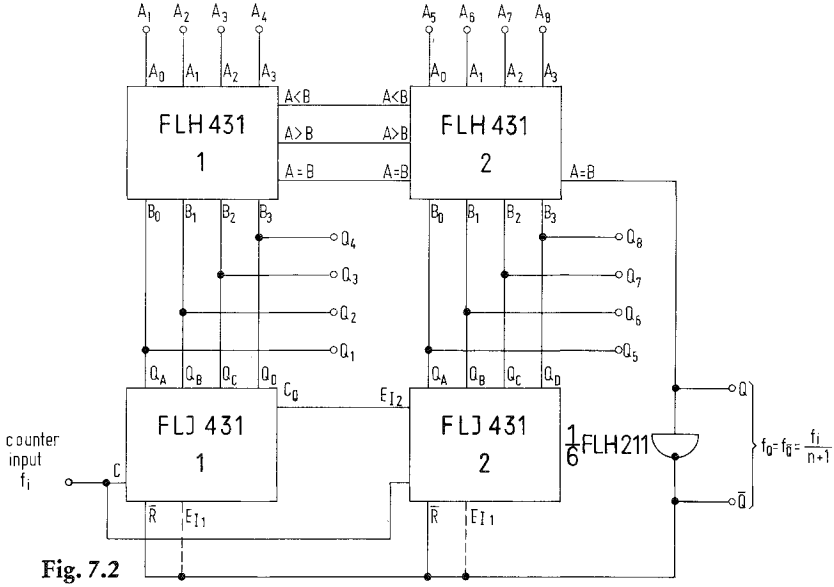


Fig. 7.2

The division ratios are achieved as follows:

Dec.	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	end of counting at	division ratio $f_Q : f_i$
0	L	L	L	L	L	L	L	L	—	1 : 1
1	L	L	L	L	L	L	L	H	2	1 : 2
2	L	L	L	L	L	L	H	L	3	1 : 3
3	L	L	L	L	L	L	H	H	4	1 : 4
4	L	L	L	L	L	H	L	L	5	1 : 5
5	L	L	L	L	L	H	L	H	6	1 : 6
⋮				⋮					⋮	⋮
15	L	L	L	L	H	H	H	H	16	1 : 16
16	L	L	L	H	L	L	L	L	17	1 : 17
17	L	L	L	H	L	L	L	H	18	1 : 18
⋮				⋮					⋮	⋮
255	H	H	H	H	H	H	H	H	256	1 : 256

The pulse at the comparator output A = B is also favourable for applications of frequency division. In this case the pulse duration corresponds to a clock cycle of pulse and interval.
If a counter reset is not required but only a stop, then the connection between the reset input $\overline{R}$ and $\overline{Q}$ has to be interrupted and a new one to be made to the enabling input E_{I1} (see dashed line). The reset may be done by a pushbotton connected to $\overline{R}$.

List of parts:
1/6 FLH 211 Q 67000-H 153
2 FLH 431 Q 67000-H 494
2 FLJ 431 Q 67000-J 279

7.3 Program controlled counter and frequency divider

Fig. 7.3 shows a counter with a division ratio n which may be set betwenn the decimal figures 2 and 16. Choice of the figure desired is made by connecting the inputs of the NAND-gate FLH 121 to X_1 to X_4. If X_3 and Q_3 as well as X_4 and Q_4 are tied together, for instance, and X_1 and X_2 not, a L-signal occurs at the reset R when Q_3 Q_4 = HH, i. e. when the 12th pulse has passed the input C of the counter FLJ 431. The reset of the FLJ 431 is clock controlled and only happens with the clock pulse n + 1. This means that 13 clock pulses are required for one cycle.

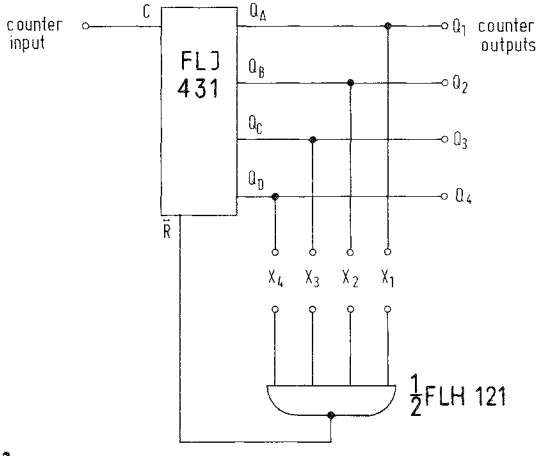


Fig. 7.3

In the following table the connections between Q and X are given for the counters desired:

X_1	X_2	X_3	X_4	end of counting at
O	O	O	O	—
G	O	O	O	2
O	G	O	O	3
G	G	O	O	4
O	O	G	O	5
G	O	G	O	6
O	G	G	O	7
G	G	G	O	8
O	O	O	G	9
G	O	O	G	10
O	G	O	G	11
G	G	O	G	12
O	O	G	G	13
G	O	G	G	14
O	G	G	G	15
G	G	G	G	16

G: connection
O: no connection

The circuit shown in Fig. 7.3 suits also for counters with asynchronous or clock independent resetting, e. g. FLJ 411. It has to be considered, however, that with this application false pulses may occur due to signal delay on reset loop. In this case the counter output remains first in that state corresponding to the preset division ratio until the reset pulse has passed through the switching circuit and the counter. The level of the counter output changes only to Q = L momentary after reaching the state for the division ratio required. These pulse peaks may create erroneous information in further stages connected and opperated by the counter output signal. This disadvantage is avoided for sure by use of the full synchronous counter FLJ 431, since the reset occurs with the clock pulse n + 1.

List of parts:

1/2 FLH 121, Q 67000-H 3
1 FLJ 431, Q 67000-J 279

7.4 Reversible control for counting circuits

The decade counter FLJ 241 as well as the binary counter FLJ 251 offer separate clock pulse inputs for up and down running. Only if both clock pulses do not coincide a proper operation of these counters is guaranteed. The circuit shown in **Fig. 7.4 a** applies to this requirement if uniform pulses with a phase displacement of $\pm \varphi$ are supplied to A and B. The signal propagation delay times of the input pulses are relatively uncritical, since a Schmitt-trigger is used. Therefore this circuit is especially favoured for applications of code-discs and optoelectronic components.

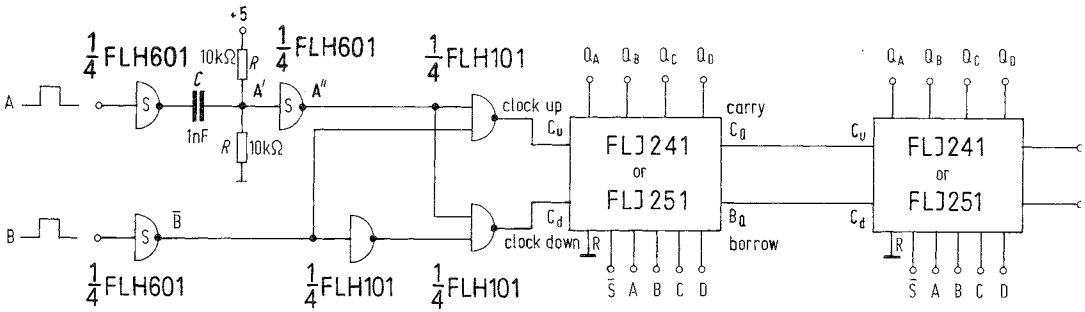


Fig. 7.4 a

The operation of this circuit is based on differentiation of the A-pulse leading edge at the RC section 10 kΩ, 1 nF and only the following Schmitt-trigger forms the real clock pulse A". The direction of counting is determined by the B-pulse. A positive shift + φ enables the clock-down input of FLH 101 and inhibits the clock-up input of this circuit. The reversed operation is achieved with a negative shift — φ. The pulse-diagrams for up and down operation are shown in **Fig. 7.4 b** and **c.**
The min. value of $\pm \varphi$ and with that the possible counting frequency depend on the time constant of the RC-section. Both may be varied in large ranges by suitable changes of the RC-values.

It has to be considered in this case that the min. admissible clock pulse duration is not to go below a value of $t_c = 20$ ns.
An extension of this counting chain is possible with additional circuits: FLJ 241, FLJ 251. With inputs A, B, C, D and $\bar{S}$ a counter preset may be achieved to a mean value.

List of parts:

3/4 FLH 101, Q 67000-H 1
3/4 FLH 601, Q 67000-H 297
2 FLJ 241 or FLJ 251, Q 67000-H 174 or Q 67000-J 175

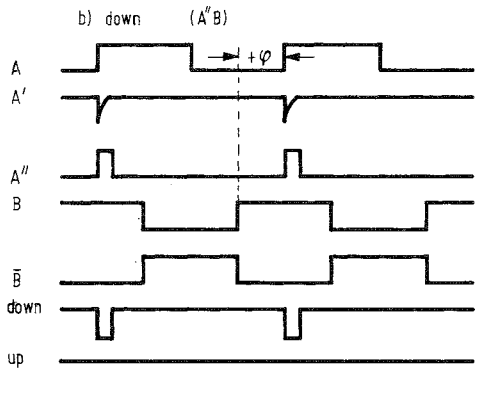


Fig. 7.4 b

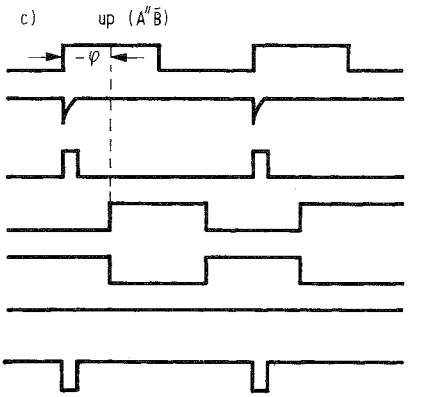


Fig. 7.4 c

7.5 Shift register with two-phase control

The output Q of a D-flip-flop level controlled follows each information change at input D, if the clock input has a high level C = H. Series operation of these circuits used in registers is only possible with the aid of a two-phase clock control as demonstrated in **Fig. 7.5.** During clock phase 1 only the clock inputs of the stages 1, 3, 5 etc receive a H-signal, whereby the inputs of stages 2, 4, 6 etc have C = L. During clock phase 2 this is vice versa, i. e. C = L applies to 1, 3, 5 etc and C = H to 2, 4, 6 etc. By this means always half of the D-flip-flops are

inhibited and the information only passes through the respective stage following. Without this two-phase control the information will pass through the register from D to Q_8.
The clock phases are generated by the flip-flop FLJ 341, which operates as a binary divider. At the same time with the generator pulse the outputs Q and $\bar{Q}$ as well as the AND-gates FLH 381 are alternately enabled. The generator pulse frequency is not to be higher than twice the value of the counting frequency f_c of the D-flip-flops.

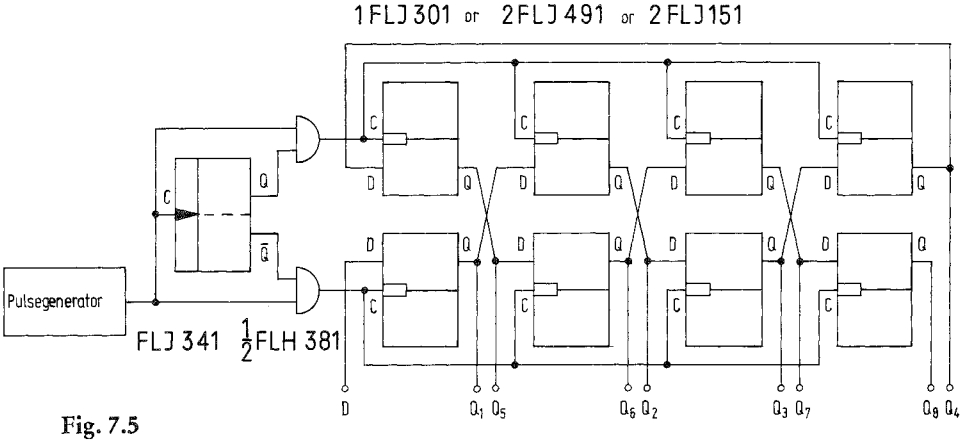


Fig. 7.5

The advantages of the two-phase technique are a better noise immunity as well as a lower dynamic power dissipation per clock pulse.

List of parts:

1 FLH 381, Q 67000-H 398
1 FLJ 341, Q 67000-J 224
2 FLJ 151 or 1 FLJ 301 or 2 FLJ 491, Q 67000-J 5 or
Q 67000-J 164 or Q 67000-H 259.

7.6 Application possibilities of the synchronous counters FLJ 201/211, FLJ 241/251 and FLJ 401/411/421/431

For construction of counting chains a lot of different possibilities of connections are offered by the circuits FLJ 201/211, FLJ 241/251 and FLJ 401/411/421/431.

The various circuits differ mainly from each other by the achievable counting frequency. In general it has to be considered that for all circuits a change of input conditions should only occur, if all pulses have passed through the total counting chain.

Fig. 7.6 a shows one of the simplest circuits using synchronous reversed counters 201/211. The operation up or down is chosen by the parallel inputs MC. The total counting chain is inhibited by a H-signal at the enabling input E_I of the 1st stage. Preset of counters is achieved at $\overline{S} = L$ independently of all other input conditions. The counters are driven in series by connecting the output E_Q and the clock input of the following stage. At the same time E_Q is also responsible for operation of the carry and the clock pulse. The signal delay between C and E_Q determines the possible clock pulse duration and thus the counting frequency. This delay created by 2 NAND-gates amounts 20 ns. Therefore the necessary clock pulse duration is the propagation delay time sum of all counting stages.

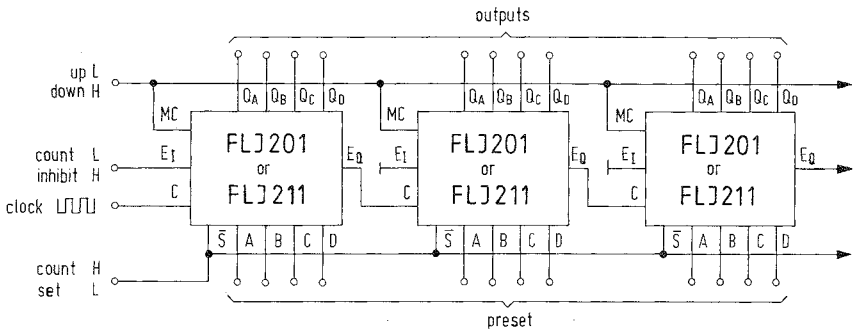


Fig. 7.6 a

Fig. 7.6 b shows a very similar counting chain with the circuits FLJ 201/211. The difference lies in the parallel clock operation and in the serial enabling. The clock pulse duration and the counting frequency depend in this application on the propagation delay between E_I and E_Q.

This delay time corresponds with the one of two NAND gates and determines the lower limit of the clock pulse duration if the delays of all stages are added up.

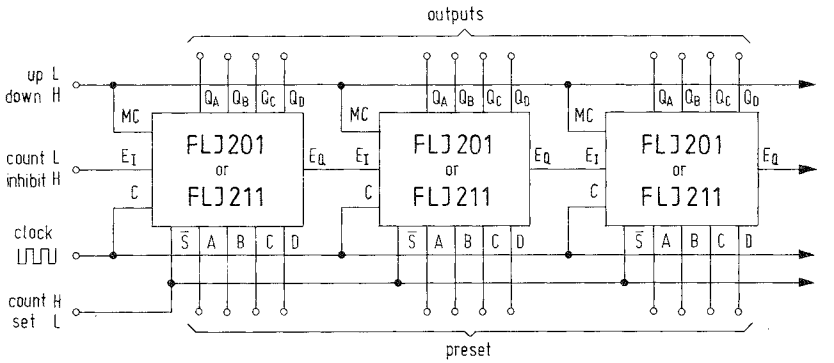


Fig. 7.6 b

Operations up to the cut-off frequency of a counter are possible with the circuit shown in **Fig. 7.6 c**. The carry is obtained with the aid of two additional NAND-gates with 1, 2, 3 etc. inputs. Already after the leading edge of the 8th clock pulse the carry pulse is available at the carry output C_Q.

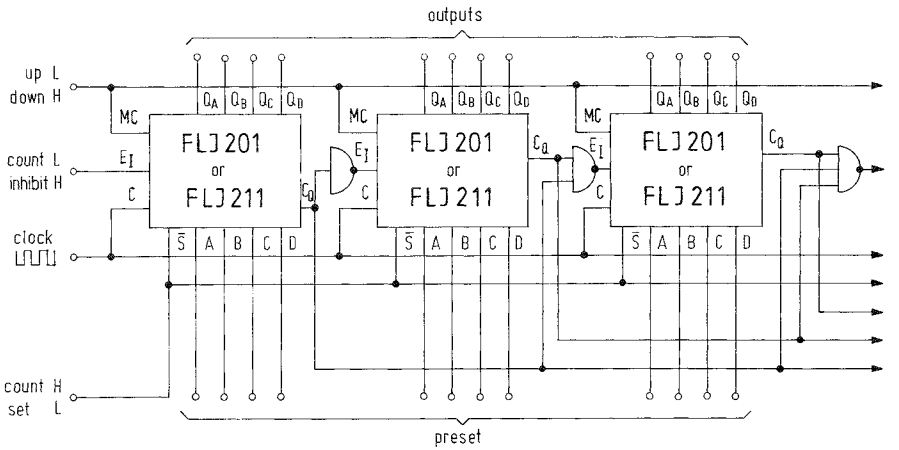


Fig. 7.6 c

By this means the following stages can be prepared during the clock interval. The number of stages is now without any influence on the clock pulse duration. Therefore the typical counting frequency $f_c = 25$ MHz of the single stages can be used to advantage. The counting chain is limited to 11 stages by the admissible load factor at C_Q of the first counter.

The synchronous reversed counters FLJ 241/251 are suited for serial counting chains as shown in **Fig. 7.6 d**. Up and down counting is controlled by the clock inputs C_u and C_d. Overlapping of the clock pulses is not allowed, as it results in indefinable counter states. The carry is serially achieved via connections C_Q—C_u and B_Q—C_d. At the same time it is also the clock pulse for the following stage. If there is a L-signal at the set input $\overline{S}$ the counters take the preset information independently of all other input conditions. Clock pulse duration and thus counting frequency are determined by the propagation delay from clock input to carry output. Its average value is 25 ns, which is determined by two NAND-gates for obtaining the carry. For counting chains it is necessary that the lower limit of the clock pulse duration is as high as the propagation delay time sum of all counting stages.

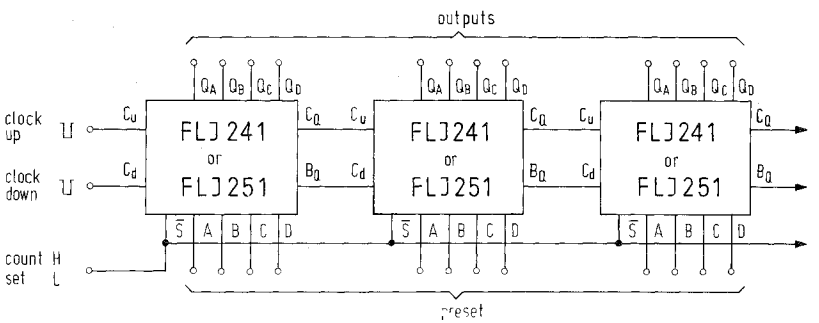


Fig. 7.6 d

The simplest circuit of a counting chain with synchronous counters FLJ 401/411/421/431 is shown in **Fig. 7.6 e**. The clock inputs C are connected in parallel. The carry is serially obtained from carry output C_Q to the enabling input E_{I2} of the following stage. The total counting chain is inhibited by a L-signal at E_{I2} of the first stage.

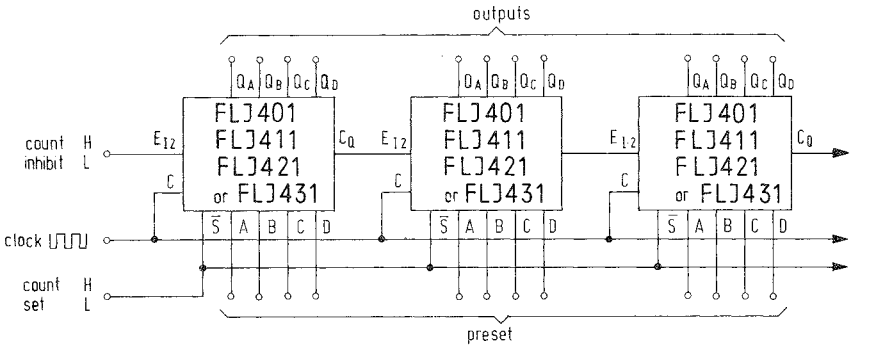


Fig. 7.6 e

If the set input $\bar{S}$ has a L-signal, the counters take the preset information during the following clock pulse. With these counters the carry is propagated at the leading edge of the 8th clock pulse, so that the following stages are enabled during the clock pulse interval. The propagation delay between C and C_Q of the first stage as well as the delay between E_{I2} and C_Q of all following stages determine the interval length. Thereby the lower limit is achieved in the state of decimal 9, when the carry pulse has to pass through all stages. Therefore the necessary clock pulse interval and thus the possible counting frequency are given by the sum of these propagation times.

The counters FLJ 401/411/421/431 offer two enabling inputs each, E_{I1} and E_{I2}. Therewith it is possible to build up counting chains with parallel carry of the first stage and with serial carry of all the following ones. As shown in **Fig. 7.6 f** the carry output C_Q is connected to the enabling inputs E_{I1} of the following stages. From stage two and followings the carry propagation is achieved as already demonstrated in Fig. 7.6 e. The advantage of this circuit is given by the essentially higher counting frequency which depends now only on the propagation time between C and C_Q of the first stage. By this means this chain can be used up to the typical cut-off frequency $f_c = 25$ MHz. However, by the output load factor permissible at C_Q this counting chain is limited to a number of 11 stages.

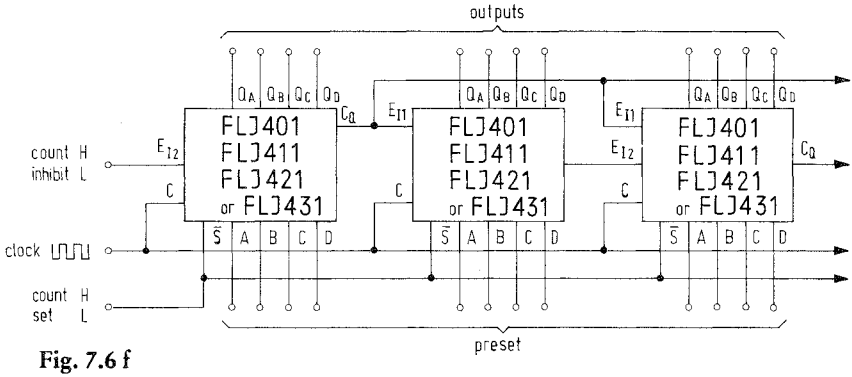


Fig. 7.6 f

List of parts

Fig. 7.6 a and b:	3 FLJ 201 or 3 FLJ 211 Q 67000-J 144 or Q 67000-J 145
Fig. 7.6 c:	3 FLJ 201 or 3 FLJ 211 Q 67000-J 144 or Q 67000-J 145 1 FLH 111, Q 67000-H 2
Fig. 7.6 d:	3 FLJ 241 or 3 FLJ 251 Q 67000-J 174 or Q 67000-J 175
Fig. 7.6 e and f:	3 FLJ 401 or 3 FLJ 411 or 3 FLJ 421 or 3 FLJ 431 Q 67 000-J 277 or Q 67000-J 273 or Q 67000-J 278 or Q 67000-J 279

8. Circuits using elements of LSL-series FZ 100

Following are some practical applications of the LSL-series FZ 100. It has to be noticed that for all IC's the connections to the power supply, having a voltage between 11 and 17 V, are not drawn. The operating voltage recommended is between 12 V and 15 V.

8.1 Noise immunity and external components

The noise-immune low speed logic series FZ 100 is favoured for those applications requiring a high static as well as dynamic noise immunity. For extremely critical situations the propagation delay times of the FZ 100-series can be increased by adding capacitors so that the dynamic noise immunity will meet the given conditions. This delaying is important in those applications where very long transmission leads exist between the signal source and the receiver. The choice of a suitable capacitor added to the receiving circuit allows the effective suppression of external noise sources. In most cases complete functional circuits are protected sufficiently, if the additional wiring is provided only at the input circuit.

With gates the capacitor is connected between N-node and output Q.

For circuits with higher integration an additional capacitor is connected between the N-node and ground. In this case the effect of noise suppression at the input is the same as that of a gate.

In comparison flip-flops FZJ 101 and FZJ 111 require two resp. four capacitors. Thus three methods of wiring are possible:

a) at the master using a capacitor each between N_J an N_J as well as between N_K and N_K,

b) at the slave with a capacitor each between N_Q and Q as well as between $\overline{N}_Q$ and $\overline{Q}$,

c) common at master and slave

In the following table the different wiring modes as well as their advantages are summarized.

Input conditions at			noise voltage at	recommended wiring as described under
T	$\bar{R}$ or $\bar{S}$	J or K		
H	H	X	$\bar{R}$ or $\bar{S}$ ↓	b
L	H	X	$\bar{R}$ or $\bar{S}$ ↓	a
H	H	X	T ↓	c
L	H	X	T ↑	a
H	H	X	J or K	a
L	H	X	J or K	not required
H	X	X	V_S	not required
L	X	X	V_S	a
X	X	X	Q or $\bar{Q}$	not required

X = L or H

↑ positive noise voltage

↓ negative noise voltage

Instead of a wiring according to methods a to c there is also a single-sided one of master and slave possible. For approximately the same effects the capacitance has to be 2 to 5 times higher than with symmetrical wiring. In this case however the unequal slopes of the switching edges are disadvantageous.

The table above shows that wiring mode b is suitable for applications of RS-flip-flops and the best noise immunity is obtained by mode c. At T = L the slave capacitors and at T = H the master capacitors receive the logic state. For less critical applications method a is sufficient in general.

The additional capacitors determine the switching times and thus the max. possible clock frequency. The following values are guidelines:

capacitance C [pF]	clock frequency f [kHz]
3000	1
300	10
20	100
0	500

The capacitance C_N is practically unlimited. According to the application of delayed flip-flops it has to be considered, that the following circuits connected to the Q-outputs also operate with delay. This is very important to know, if counter outputs are decoded. Output pulse overlapping of the different counter outputs are avoidable, only if the

relevant decoding circuit is also delayed. The recommended ratio of the capacitors at the flip-flop slave C_{NF} to the capacitors at the gate C_N is: C_{NF} to C_N = 1 to 4.

8.2 Hints for system configuration

Fig. 8.2 a shows a proposed circuit for a digital control configuration including the system parts: signalling, control logic, power matching, power stage and power supply.

Unlike mechanical systems, it is necessary in designing electronic digital control systems to proceed from the assumption that their functioning is liable to be impaired by noise voltages. Such voltages may be either pulses produced, say, as the result of an unfavourable interconnection pattern, or may be picked up from outside the system, whereby the extent of the external noise voltages at the site of the system is often unknown and the first problems arise after the system has been commissioned. The system should therefore be so designed that noise voltages will be intercepted before reaching the logic assembly. Noise suppression at the input is here of particular importance. Our LSL series offers a large degree of freedom in this respect by allowing the addition of noise suppression capacitors. Provision is made for these capacitors at the planning stage and, if necessary, they can be adapted to the existing conditions on site. Guidelines for practical system design will be given in the following.

8.2.1 Power supply

The use of separate power supplies and leads for feeding the various parts of the system offers the optimum solution. This sectionalization precludes the possibility of the noise infestation of other parts of the system as might occur, say, if a rise in current in the power section were to cause voltage drops across a common reference lead.

Effective immunity to RF noise superimposed on the line ac voltage is provided by a primary side line voltage filter. Although such filters are not always necessary, they reduce the danger of malfunctions. The B81931A . . . series is among the suitable types.

Large fluctuations in line voltage and load current can only be compensated with a voltage regulator. To minimize the effect of changes in load current, the internal resistance R_i should be less than 1 Ω.

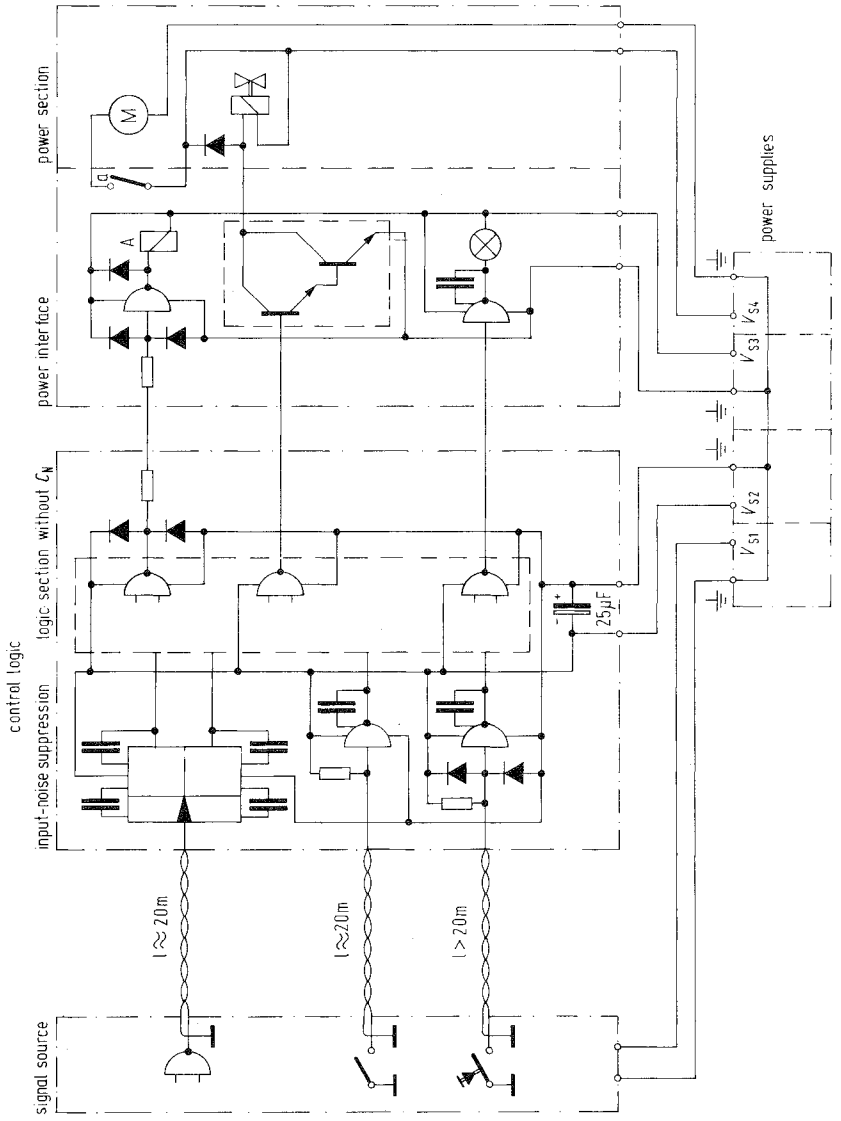

control logic
power section
power interface
logic section without C_N
input-noise suppression
signal source
power supplies
M
A
25µF
V_{S1}
V_{S2}
V_{S3}
V_{S4}
l ≈ 20m
l ≈ 20m
l > 20m

Fig. 8.2

Provided that the load current of the LSL system does not vary during operation by more than a certain extent, a power section consisting of a transformer, a bridge rectifier and a charging capacitor will be sufficient. For example:

The functioning of LSL systems is assured over a supply voltage range V_S of 11.4 to 17 V; the AND-OR gate FZH 151 still functions at a voltage V_S of 10.5 V. Optimum utilization of this voltage range is possible by choosing a supply voltage of intermediate value, i. e. 14.5 V. The commonly permissible line ac voltage fluctuation is —15 % and + 10 %. Referenced to $V_S = 14.5$ V, a lower supply voltage of 12.3 V and an upper value of 16 V result. This leaves a margin of $\triangle V = 1$ V from the associated limit which can be used as a voltage drop in the case of changes in the load current ΔI. If ΔI is known, the required dynamic internal resistance R_i of the power supply calculates at $\Delta V : \Delta I$. In the case of an unregulated supply, the resistance R_i depends largely on the chosen transformer. For switching operations the changes in load current are of the order of microseconds. The reduction of the internal resistance by the charging capacitor is still assured at this speed. Empirical values for the internal resistance of power packs are, for instance, $R_i \approx 5\ \Omega$ for a transformer core M65 with a bridge rectifier rated for 14.5 V and 1 A. The permissible change in load current is in this case

$$\Delta I = \frac{\Delta V}{R_i} = \frac{\pm 1\ \text{V}}{5\ \Omega} = \pm 0.2\ \text{A}.$$

Typical guideline values for the change in load current ΔI relative to the average operating current I are 20 to 30 %. If a safety margin of 10 % is allowed for, the permissible current values are 500 to 700 mA. A power pack such as this is suitable for the operation of 300 gates, 50 flip-flops or a corresponding combination of both. The charging capacitor should have a capacitance of about 2 to 3 mF. A 1 nF ceramic capacitor should be connected in shunt with the charging capacitor for suppressing RF noise pulses. If the M65 core is replaced by a M85A core and all other conditions are the same, the stated values will be doubled.

Circuits with the FZH 241 Schmitt trigger need, if an unregulated power supply is used, a 1 µF capacitor, which should be mounted as close to the terminals of the package as possible.

8.2.2 PC board

LSL elements do not produce any undesired signal crosstalk. The length, spacing and layout of the signal transmission leads on the PC board can therefore be chosen arbitrarily. To assure the positive avoidance of coupling noise and mode excitation, the leads to the N-terminals of LSL elements must not be longer than 5 cm. Links between the function inputs of the FZK 101 timing circuit must not be longer than 5 mm and the leads to its RC sections should be kept as short as possible.
The layout of the leads to points V_S and O_S is not critical if only LSL elements have to be fed. A capacitor with a capacitance $C \geqq 10$ µF will improve the protection of the standard European PC board from short-term voltage dips. If additional load currents from relays and lamps mounted on the same board flow through the supply leads, a meshed lead system will be necessary. Owing to its favourable constructional design and low cost, the use of this system is generally recommendable.

8.2.3 Rack wiring

Owing to the high permissible mutual capacitance of two signal transmission lines, LSL elements allow flexibility in wiring routes. Only long leads with an unfavourable path may have to be protected by choosing elements with a wired N-terminal. For further details please refer to section 8.2.5. A rack power supply lead network of low impedance with thick ground wires or ground plates will reduce the danger of external noise pickup.

8.2.4 Cabinet design

In the cabinet the signal transmission lines must be protected according to their length and locating as described in the next section. These measures are particularly important if the cabinet also accommodates thyristors, triacs, motors, relays, contactors and other sources of serious RF noise.

A ground bar is required for ground potential. All ground and RF shielding leads must be connected to the ground bar by short low-impedance leads. Line voltage leads in the cabinet, as also the input and output leads of the power and control sections, must be RF shielded. The control electronics must be isolated from the case to avoid noise pickup.

8.2.5 Signal transmission and noise immunity

The following likewise applies to the cabinet design, the rack wiring and the LSL transmission lines.

Since the possible length of a signal transmission line depends mainly on the noise level and the associated changes in potential, it is always advantageous to choose shielded cables with twisted pairs for all transmission lines of over 10 m in length. Undesired electromagnetic effects are in this case largely suppressed. Twisted signal transmission and ground wires provide increased protection from strong RF interference fields.

For n mutually interfering gates without a wired N-terminal, the following transmission line lengths l have been empirically determined:

n	l [m]
2	~ 30
5	~ 10
10	~ 5

With the N-terminal wired, transmission lines of over 100 m in length have already been realized.

The noise immunity of LSL elements to external noise pickup was tested using a noise simulator. Fluorescent tubes were turned on, contactors operated, differentiating pulses produced and LSL signals transmitted over a wire line 20 m in length run alongside a disturbing parallel line. The insertion of a 1 nF capacitor C_N already provided noise immunity. The appropriate circuit configurations are shown in **Fig. 8.2 a** and **b.**

The configuration shown in **Fig. 8.2 c** is suitable for line lengths of over 20 m under conditions of extreme noise. The BAY 60 diodes protect the LSL element from destruction by sharp positive and negative voltage spikes. The dynamic noise immunity is adjustable

with capacitor C_N. The following capacitances are sufficient to suppress noise pulses up to a pulse duration t:

C_N	t
1 µF	10 ms
100 nF	1 ms
10 nF	100 µs
1 nF	10 µs
100 pF	1 µs

The permissible noise pulse duration can be lengthened by increasing the capacitance. In practice, however, noise pulses of longer than 5 ms are hardly to be expected. The Schmitt trigger S supplies pulses with an adequately short rise time at subsequent dynamic inputs. **Fig. 8.2 d** shows the noise immunity behaviour.

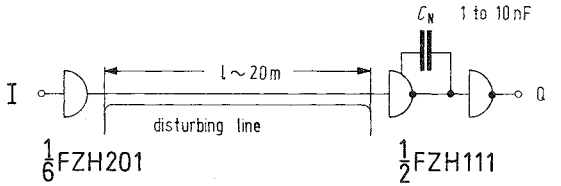


Fig. 8.2 a

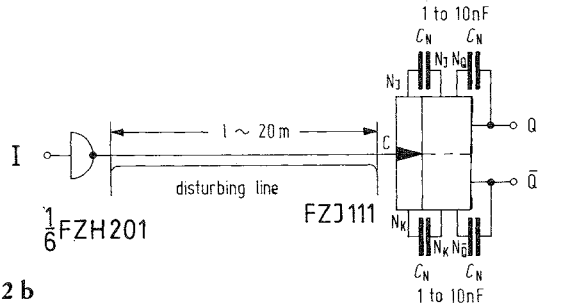


Fig. 8.2 b

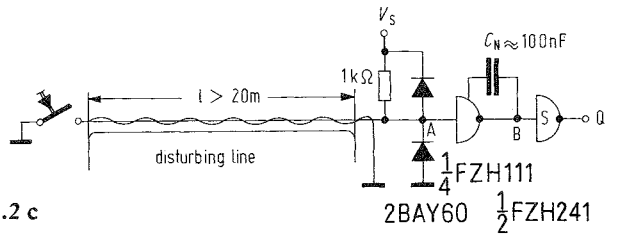


Fig. 8.2 c

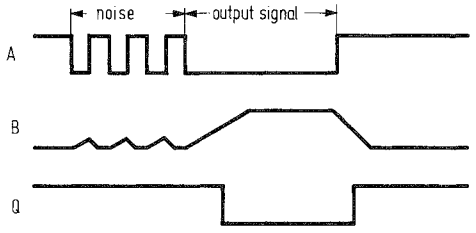


Fig. 8.2 d

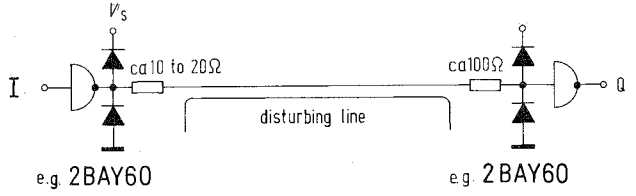


Fig. 8.2 e

Storage elements need careful consideration because RF noise at the inputs and also via the supply is liable to produce permanent misinformation. Here again wiring the N-terminal assures effective protection from inductive or capacitive noise on the supply leads. (See also section 8.1) Fig. 8.2 b shows a suitable configuration for flipflops. With flipflops, which consist of crosscoupled NAND-gates, the insertion of a capacitor $C_N = 1$ to 10 nF at one gate is usually sufficient. Logic elements without a wired N-terminal (FZJ 131) and with a permissible N-capacitance of $C_N < 500$ pF (FZJ 141, FZJ 151, FZJ 161 and FZK 101) can be additionally protected by shunting the terminals V_S and O_S with a capacitor $C_N = 10$ to 100 nF. The wired N-terminal is further suitable for suppressing contact bounce. C_N should then be chosen between 10 and 100 nF, depending on the bounce frequency.

As a general rule it may be said that the unassigned inputs of simple gates and flipflops may be left open. Since the functioning of counters, shift registers and other elements with a higher scale of integration is only assured at a definite input potential, inputs not required in operation should be connected via a protective resistor $R = 1\,\text{k}\Omega$ to the supply voltage.

Input lines which are temporarily opened by, say, a relay contact, should always be avoided as being a too frequent source of noise. The remedy is to interpose a resistor $R = 1\ k\Omega$ between logic elements and the supply voltage V_S (Fig. 8.2 c).

8.2.6 Proposal for system configuration

Fig. 8.2 shows a digital machine control system configuration comprising separate sections for signal generation, control logic, power interface, power section, and voltage supply. Interference to the flow of signals is to be expected along the transmission paths between signal generation and control logic as well as at the control logic and power interface. Since noise in the input lines is particularly critical when storage-type devices follow, the primary function of the control logic is to separate the output signals from the noise. LSL elements here offer an extremely economic solution because they allow the addition of capacitors of any size. If the noise is filtered out, the N terminal of the logic section need not be wired unless other noise sources are present (as shown in Fig. 8.2). Control logic sections with transmission lines over 100 m in length have already been realized by this means. The choice of a capacitor of appropriate size is here decisive. A useful guideline value for such transmission lines is $C_N > 100$ nF.

The transmission of clock signals over a long line is basically possible as described in section 8.2.5. Since however there is a serious risk of misinformation, the line length should be limited to 20 m. Once again the choice of a capacitor of appropriate size is decisive. Favourable values are $C_N = 1$ to 10 nF.

There is no danger of RF noise pickup with motors, electromagnets, lamps, heating equipment and other power elements with a large time constant because they react almost only to static signal changes. Since the power interface section contains no storage elements which could produce permanent misinformation, the protection of this transmission path from noise by wiring the N terminal is unnecessary. Although short noise pulses pass through the gates, the power elements do not respond to them. The length of the transmission path is relatively uncritical.

If extreme voltage spikes appear it is further necessary to protect the LSL inputs from destruction. The amount of energy permissible at the input or output without danger of destruction is here typically 1 mWs. **Fig. 8.2 e** shows a suitable protective circuit. Noise pickup is removed by way of diodes. The series resistors provide adequate current limitation.
The various sections of the system are fed over separate power leads, so avoiding powerline couplings as already noted in 8.2.1.

8.3 Bidirectional counters

8.3.1 Binary bidirectional counter

Fig. 8.3.1 shows a synchronous bidirectional counter with binary coded preset obtained at inputs A_1 to A_4. By opening the set push button the respective gate inputs are enabled with a H-signal. The input condition A = L gives $\overline{R}$ = L at the reset input due to the dual inversion and $\overline{S}$ = H at the set input on account of the single inversion. Thus the flip-flop FZJ 121 is set to Q = L. Under the condition A = H a preset to Q = H is performed. The set operates independently of all other input conditions of the reversible counter, since the $\overline{R}$ and $\overline{S}$ inputs of the FZJ 121 have priority.
The operation mode is chosen by the input BA. For upcounting it has to be: BA = H. Thus the NAND-gates connected also to outputs Q_1, Q_2 and Q_3 are enabled and the NAND-gates driven by the inverter FLH 201 are inhibited. The JK information of the second flip-flop thus corresponds to the state at Q_1. At the third stage it is JK = $Q_1 \bigwedge Q_2$ etc. Down counting is achieved at BA = L; the JK-conditions now being derived from the $\overline{Q}$-outputs.

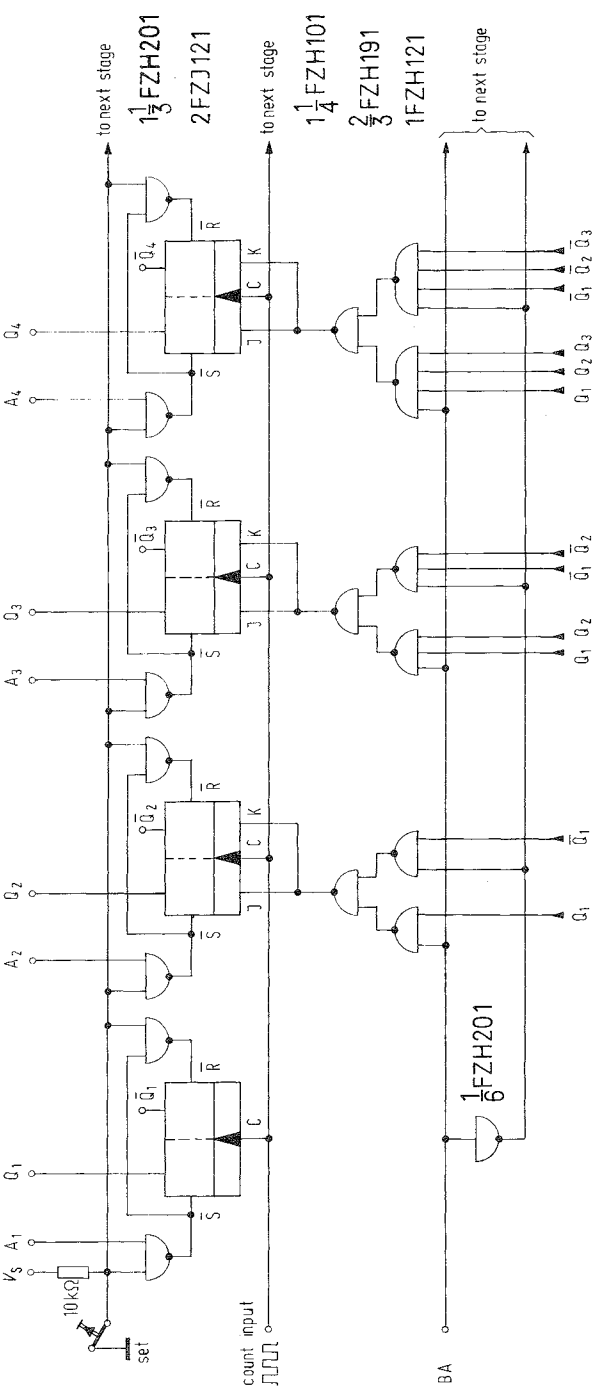

to next stage
1 1/3 FZH201
2FZJ121
to next stage
1 1/4 FZH101
2/3 FZH191
1FZH121
to next stage
1/6 FZH201
V_S
10 kΩ
set
count input
BA
A_1 A_2 A_3 A_4
Q_1 Q_2 Q_3 Q_4
$\bar{Q}_1$ $\bar{Q}_2$ $\bar{Q}_3$ $\bar{Q}_4$
S R C J K
Q_1 $\bar{Q}_1$
Q_1 Q_2 $\bar{Q}_1$ $\bar{Q}_2$
Q_1 Q_2 Q_3 $\bar{Q}_1$ $\bar{Q}_2$ $\bar{Q}_3$

Fig. 8.3.1

The truth-table for the counter is as follows

up-operation						
pulses at counter input	mode of operation BA	outputs Q_4 Q_3 Q_2 Q_1				decimal figure corresponding
1	H	L L L L	L	17		0
2	H	L L L H	L	16		1
3	H	L L H L	L	15		2
4	H	L L H H	L	14		3
5	H	L H L L	L	13		4
6	H	L H L H	L	12		5
7	H	L H H L	L	11		6
8	H	L H H H	L	10		7
9	H	H L L L	L	9		8
10	H	H L L H	L	8		9
11	H	H L H L	L	7		10
12	H	H L H H	L	6		11
13	H	H H L L	L	5		12
14	H	H H L H	L	4		13
15	H	H H H L	L	3		14
16	H	H H H H	L	2		15
17	H	L L L L	L	1		0
		Q_4 Q_3 Q_2 Q_1 outputs	BA mode of operation	pulses at counter input		
		down operation				

An extension of the counter is easily possible by using the following rule for JK-conditions.
It applies for up-operation:

$$JK_n = Q_1 \wedge Q_2 \wedge Q_3 \wedge Q_4 \wedge \ldots Q_{n-1}$$

and for down-operation:

$$JK_n = Q_1 \wedge Q_2 \wedge Q_3 \wedge Q_4 \wedge \ldots Q_{n-1}$$

List of parts:

1 1/4 FZH 101, Q 67000-H 190
1 FZH 121, Q 67000-H 192
2 FZH 191, Q 67000-H 633
1 1/2 FZH 201, Q 67000-H 636
2 FZJ 121, Q 67000-J 385

8.3.2 Decimal reversible counter

With regards to a minimum quantity of components this reversible synchronous counter has been devised (refer to **Fig. 8.3.2**). The additionally required JK-inputs of the flip-flops FZJ 121 are obtained by a combination of diodes BAW 76.

The operating mode is chosen by input BA. For up-counting it applies BA = H. Thus the NAND-gates connected with outputs Q_1, Q_2 and Q_3 are enabled and control the JK-inputs of the following flip-flops FZJ 121. The NAND-gates operated by the inverter FZH 201 are inhibited. Down counting is achieved at BA = L; the JK-conditions now being derived from the Q-outputs.

The truth table is as follows:

up-counting

pulses at counting input	operating mode	carry	outputs							respective decimal figure
	BA	C	Q_4	Q_3	Q_2	Q_1				
1	H	L	L	L	L	L	H	L	11	0
2	H	L	L	L	L	H	L	L	10	1
3	H	L	L	L	H	L	L	L	9	2
4	H	L	L	L	H	H	L	L	8	3
5	H	L	L	H	L	L	L	L	7	4
6	H	L	L	H	L	H	L	L	6	5
7	H	L	L	H	H	L	L	L	5	6
8	H	L	L	H	H	H	L	L	4	7
9	H	L	H	L	L	L	L	L	3	8
10	H	H	H	L	L	H	H	L	2	9
11	H	L	L	L	L	L	H	L	1	0
			Q_4	Q_3	Q_2	Q_1	C	BA	pulses at counting input	
			outputs				carry			

down-counting

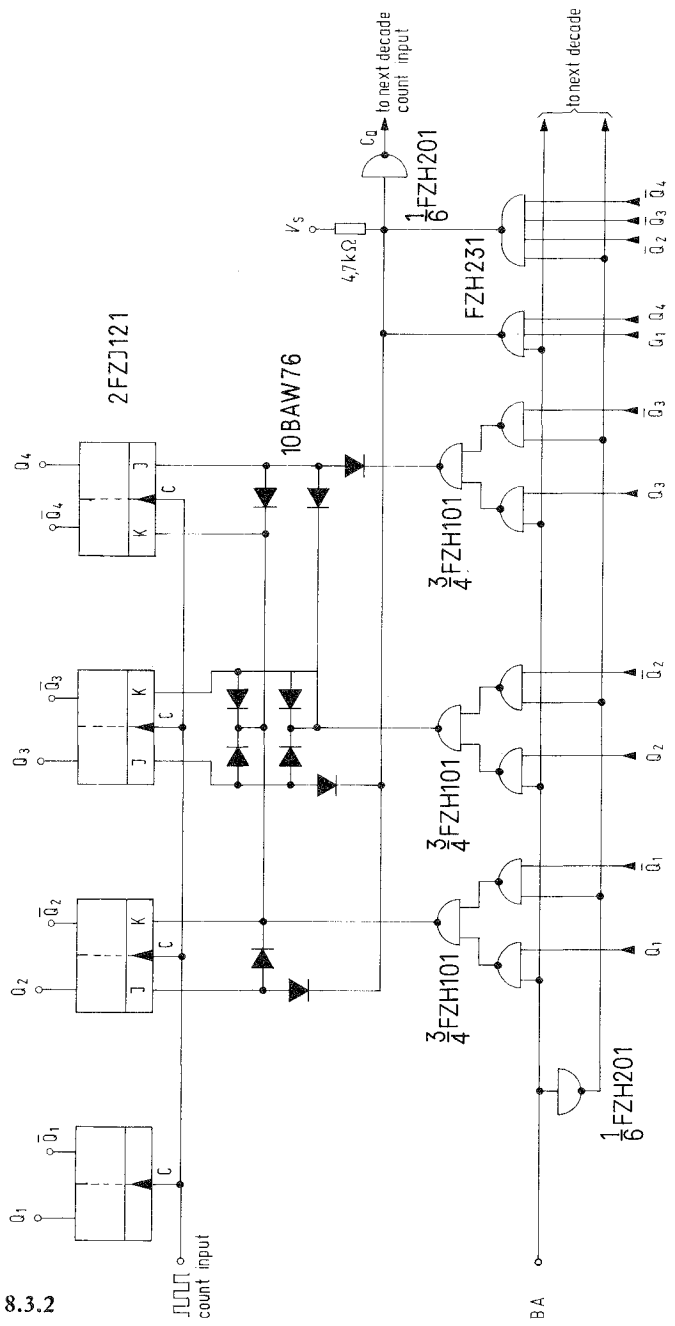

2FZJ121
10BAW76
FZH231
1/6FZH201
3/4FZH101
3/4FZH101
3/4FZH101
1/6FZH201
4,7kΩ
V_S
C_Q
to next decade count input
to next decade
count input
BA

Fig. 8.3.2

The "carry" pulse is propagated by the gate FZH 231. This pulse controls not only the counting input of the following decade but inhibits also with J = L the second and third stage being in state $Q_2\,Q_3$ = LL. This is necessary during up-counting, since due to conditions Q_1 = = JK = H a state change of the second stage is possible, when the counter changes from $Q_4\,Q_3\,Q_2\,Q_1$ = HLLH to LLLL (decimal 9 to 0). During down counting the same happens for the second and third stage, when the outputs change from $Q_4\,Q_3\,Q_2\,Q_1$ = HHHH to LHHL, which corresponds to a change from decimal 0 to 9.

Counter preset is possible by the gate FZH 201 via the RS-inputs of the flip-flop FZJ 121, as already described in 8.3.1.

List of parts

2 1/4	FZH 101, Q 67000-H 190
1/3	FZH 201, Q 67000-H 636
1	FZH 231, Q 67000-H 642
2	FZH 121, Q 67000-J 385
10	BAW 76, Q 62702-A 397

8.3.3 Decimal bidirectional counter with high noise immunity

The circuit shown in **Fig. 8.3.3** was devised with special regard to strong noise conditions. The difference to the circuit of 8.3.2 exists in the use of the flip-flop FZJ 111 instead of FZJ 121. For FZJ 111 additional wiring is possible in order to increase the dynamic noise immunity to match existing conditions. Storage of false information and false functions created from that are avoided by sure. For practical applications the additional capacitors have a value of up to 3000 pF theoretically not limited. Besides that the counter propagation delay time is shortened.

The truth table is in accordance to instructions given in chapter 8.3.2.

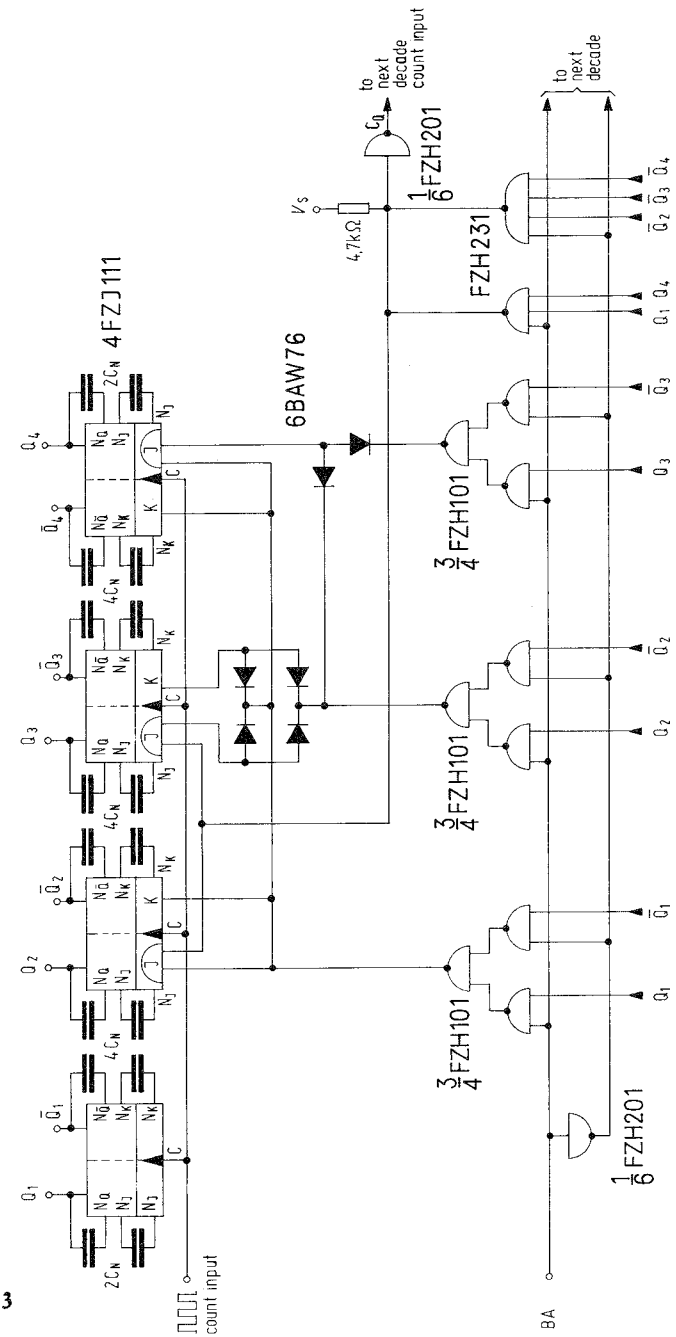

4FZJ111
6BAW76
FZH231
$\frac{1}{6}$FZH201
$\frac{3}{4}$FZH101
$\frac{3}{4}$FZH101
$\frac{3}{4}$FZH101
$\frac{1}{6}$FZH201
4,7kΩ
V_S
to next decade count input
to next decade
count input
BA

Fig. 8.3.3

Counter preset is possible by the gate FZH 201 via the RS-inputs of the flip-flop FZJ 111 as already described in 8.3.1.

List of parts:

2 1/4 FZH 101, Q 67000-H 190
1/3 FZH 201, Q 67000-H 636
1 FZH 231, Q 67000-H 642
4 FZJ 111, Q 67000-J 96
6 BAW 76, Q 62702-A 397

8.4 Matching circuits

8.4.1 Operation using the opto coupler CNY 17

Opto couplers offer many important features not possible with other sensors, for instance switching without chatter, operation free of maintenance, high life time, electrical separation at insulating voltages of up to 2.5 kV and low noise immunity.

Operation of the opto coupler CNY 17 is achieved with a few additional components only (see **Fig. 8.4.1**). It is driven by a NAND-gate with open collector, FZH 211. The resistor R = 1 kΩ determines the diode current of $I_{ph} \sim 10$ mA at $V_S = 12$ and of $I_{ph} \sim 13$ mA at $V_S = 15$ V.

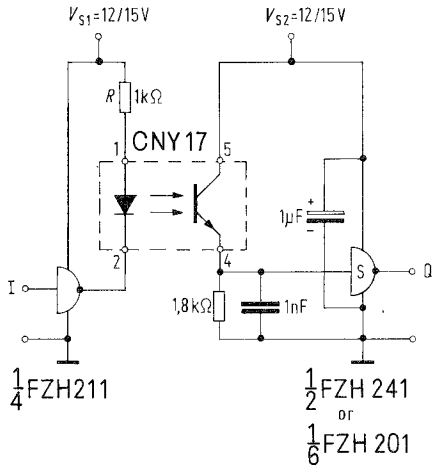


Fig. 8.4.1

Depending on the operating voltages used the collector current of the receiver transistor amounts I_C = 4 to 5 mA, i. e. a reliable operation of the coupler at an efficiency of 40 % according to group I.

The capacitor of 1 nF is used for noise suppression. This is of great importance when the photodiode is not driven by a LSL-circuit, but by a mechanical contact. Chattering is safely avoided by the choice of a suitable capacitance.

The Schmitt-trigger FZH 241 provides a sufficient edge steepness for operation with dynamic inputs, e. g. clock inputs of flip-flops and counters. The capacitor of 1 µF smoothes large power supply voltage drops, generated by switching the Schmitt-trigger. In general this measure is necessary only for operating voltages not regulated. If the requirements for edge steepness are not too strong, the Schmitt-trigger FZH 241 may be replaced by an inverter FZH 201. This change also obviates the need for the 1 µF-capacitor.

List of parts:

1/4 FZH 211, Q 67000-H 639
1/2 FZH 241 or 1/6 FZH 201, Q 67000-H 645 or Q 67000-H 636
1 CNY 17, Q 62703-N 1

8.4.2 Switching amplifier for 100 to 300 V

The switching amplifier shown in **Fig. 8.4.2** is favoured for output voltages of V_L = 100 to 300 V at load currents up to I_L = 0.5 A. The load is turned on by the power transistor BUY 35, when a H-Level is applied to the input E of the inverter FZH 201. For inductive loads a diode should be used for protection.

The load current is determined by the value of the resistor R which should be optimally matched to the required load in order to keep its power dissipation low. The values of R = 8.2 kΩ and P = 2 W as specified in Fig. 8.4.2 enable a load current of $I_L \sim 0.3$ A. The limit is I_L = 0.5 A and at this value it is R = 3.3 kΩ and P = 5 W.

The voltage drop across the conductive transistor BUY 35 is about 3 to 4 V. For currents up to $I_L < 0.3$ A it is not necessary to eliminate the generated power dissipation by a cooling block, whereas a heat sink with a thermal resistance of $R_{th} = 30\frac{K}{W}$ is indispensable for currents between $I_L = 0.3$ and 0.5 A.

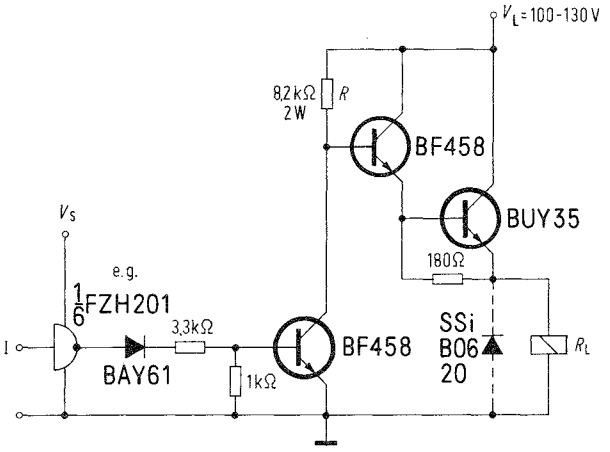


Fig. 8.4.2

List of parts:

1/6 FZH 201, Q 67000-H 636
2 BF 458, Q 66702-F 316
1 BUY 35, Q 62702-U 112
1 BAY 61, Q 62702-A 389
1 SSi B 0620, C 66047-A 1006-A 3

8.4.3 Short-circuit-proof switching amplifier for a solenoid valve

Fig. 8.4.3 shows a switching amplifier suitable for commercial soleniod valves ($V = 24$ V, $I = 0.5$ A, $R \sim 56\ \Omega$ and $L \sim 50$ mA). The power output stage is equipped with a Darlington transistor BDY 88, operating the solenoid when a L-signal is applied to the input I of the inverter FZH 201.

If a short-circuit occurs between the supply voltage terminal V_L and the collector of BDY 88 the transistor BCY 58 protects the power Darlington circuit against overloads. A voltage drop is generated at the emitter resistor R_E by the short-circuit current I_K, which turns the transistor BCY 58 on as soon as the base-emitter-voltage is attained.

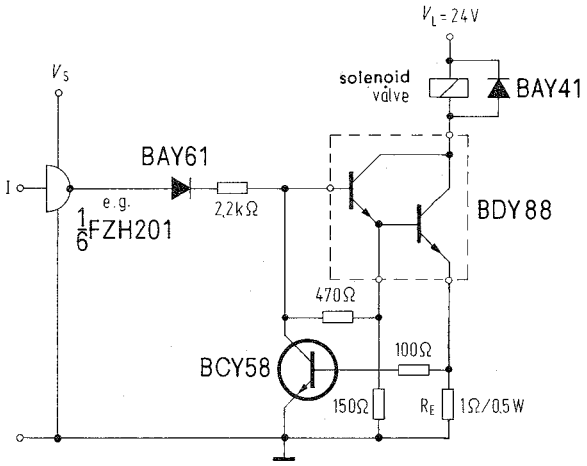


Fig. 8.4.3

The short-circuit current can be given as follows:

$$I_K \sim \frac{V_{BE}}{R_E} \text{ [A]}$$

To switch the transistor BCY 58, a V_{BE}-value of about 0.55 V is necessary; therefore the resistor R_E has to be demensioned in the way that the short-circuit current generates exactly this voltage drop. On the other hand the voltage drop created by the nominal current has to be sufficiently lower. An approximate value is given by the relation: $I_K = 1.1 \times I_N$.

Thus the resistor R_E is calculated as follows:

$$R_E \sim \frac{V_{BE}}{1.1 \times I_N} = \frac{0.55}{1.1 \times 0.5} = 1\ \Omega$$

The seize of the heat sink and the short-circuit power dissipation determine the short-circuit time. Thereby the power dissipation is approximately evaluated:

$$P_K \sim I_K \times V_L \sim \frac{V_{BE}}{R_E} V_L = \frac{0.55}{1} 24 = \underline{13\ W}.$$

From this follows that the thermal resistance of the heat sink required for the short-circuit application is:

$$R_{th} = 5 \frac{K}{W}.$$

The circuit shown in Fig. 8.4.3 is applicable for nominal currents up to approx. 1 A. In this case the short-circuit power dissipation results in a value of $P_K = 25.5$ W. From this follows for the thermal resistance of the heat sink required for a constant short-circuit current:

$$R_{th} = 1.6 \frac{K}{W}.$$

Provided that the short circuit is not repeated and does not last longer than 10 s it has been experienced that the thermal resistance can be 2 or 3 times higher than calculated above. However a trial run is suggested in all of these cases.

List of parts:

1/6 FZH 201, Q 67000-H 636
1 BCY 58, Q 60203-Y 58
1 BDY 88, Q 62702-D 130
2 BAY 41, Q 60201-Y 41

8.5 Synchronous decimal counter for 3 decades with preset

Fig. 8.5 shows a counting chain with preset. The preset inputs $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, and the reset input $\overline{R}$ operate directly and have to have a H-signal during counting. This is achieved by connecting the hexinverter FZH 201 between the pushbutton and the preset inputs. The connected strobe inputs are driven by a gate FZH 101 via a RS-flip-flop which suppresses chattering of the preset-pushbutton. In steady state the strobe inputs inhibit the inverter by L-signal. The strobe inputs change to H-signal when the pushbutton is operated. The BCD-information preset by the thumb-wheel switch V 42264 D 2 . . isswitched to the

inputs $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$. At the same time the preset-pushbutton triggers the monostable flip-flop FZK 101 for resetting the counter FZJ 141. This is necessary, since only L-levels are operative at the preset inputs $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ and switch the outputs Q to H-level.

The counter outputs are reset to Q = L by R = L. Therewith a carry transfer free of errors is only assured if set and reset inputs have L-level in common during a time of t = 1 µs and thereafter the reset input returns to H-level at least 1 µs earlier than the preset input. These conditions are guaranteed by the monostable flip-flop. The adjusted delay time is $t_M = 0.7 \times RC = 0.7 \times 15 \times 10^3 \times 0.1 \times 10^{-9} =$ 1 µs. Thus after run of this time the reset input returns to H-level, whereas the BCD-information is applied to $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ as long as the reset-pushbutton goes back to its state of rest.

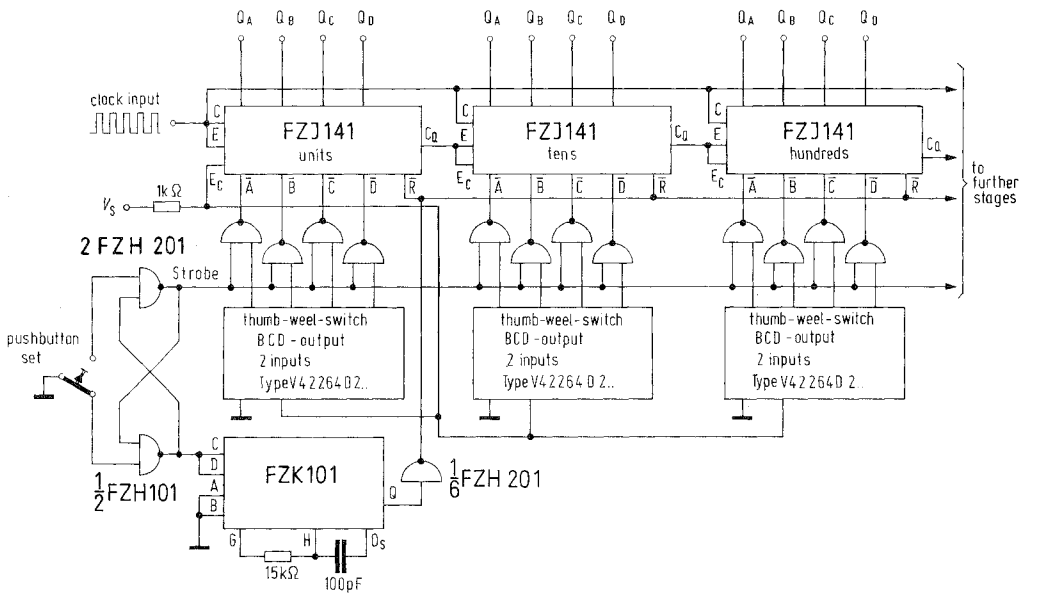


Fig. 8.5

The clock-inputs of the counting stages for units, tens and hundreds are operated in parallel or synchronously. The following stages are enabled via the connection between carry output C_Q and clock enabling input E resp. carry enabling input E_C.

If desired this counting chain can be extended in accordance with the shown pattern, whereas it has to be considered that the load factors of the RS-flip-flop driving the NAND-gate FZH 101 and the inverter FZH 201 connected to output Q of the FZK 101 are not exceeded. Not used inputs of the counters FZJ 141 have to be connected to a defined H-level, otherwise the correct function of the counters are not guaranteed. In Fig. 8.5 this applies to the carry enabling input E_c the first stage which is connected to the supply voltage V_S via a resistor R = 1 kΩ for protection. Operation of the counter FZJ 141 is possible for typical clock frequencies up to 2 MHz. The circuit shown is also applicable for the binary counter FZJ 151.

List of parts:

1/2 FZH 101, Q 67000-H 190
2 1/6 FZH 201, Q 67000-H 636
3 FZJ 141, Q 67000-J 391
1 FZK 101, Q 67000-K 6
3 thumb-wheel-switch, V 42264-D 12-A 011
1 pushbutton, C 42315-A 60-A 3

8.6 Circuit for functional extension of the timer FZK 101

Addition of external components to the timing circuit FZK 101 is limited to values of R_t = 5 to 500 kΩ. Therefore greater time constants require higher capacitances. Fig. 8.6 shows an additional circuit avoiding this disadvantage and favouring for all operating modes.

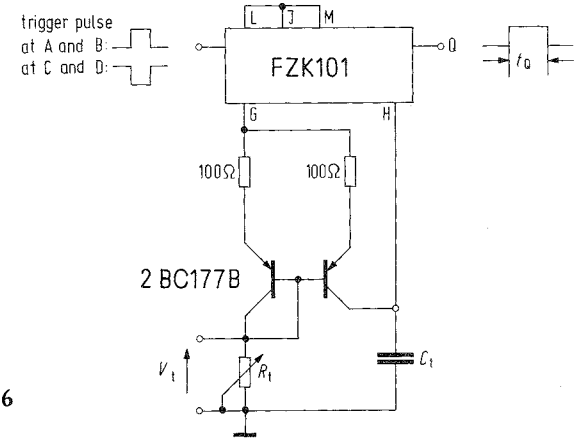


Fig. 8.6

The permissible resistance range is extended to a lower limit of R_t = 1 kΩ and to a higher one of R_t = 10 MΩ. In **Fig. 8.6 a** the resulting output pulse duration at monostable operation mode $t_Q = f(R_t)$ is shown. The parameter is C_t with values between 1 nF and 10 µF. The relation $t_Q = 0.7 \times R_t \times C_t$ [s] for calculating the output pulse duration is not effected by this additional circuit arrangement.

If the resistor R_t is replaced by a constant-voltage source V_t with a low internal impedance, then the output pulse duration t_Q is variable and depends on this voltage. The equivalent resistance $R'_t = 0.7 \times R_t$ as a result of a certain voltage is shown in **Fig. 8.6 b.** If the voltage is for instance V_t = 3 to 4 V it follows $R'_t = 0.7 \times R_t$ = 1.6 to 3.2 kΩ. Assumed that C_t is 1 nF the output pulse duration may be varied as follows:

$t_{Q1} = 0.7 \times R_t \times C_t = 1.6 \times 10^3 \times 10^{-9} =$ **1.6 µs**

$t_{Q2} = 0.7 \times R_t \times C_t = 3.2 \times 10^3 \times 10^{-9} =$ **3.2 µs**

resp. t_{Q1} to t_{Q2} = 1 to 2

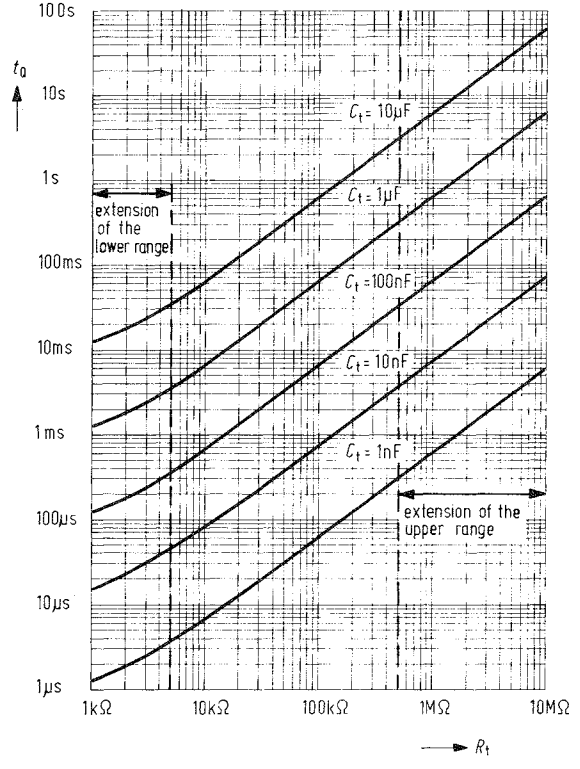


Fig. 8.6 a

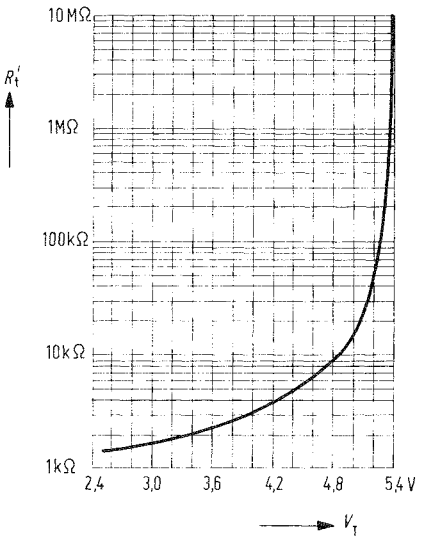


Fig. 8.6 b

The additional circuit operates as a constant-current source in the way that the current flowing through resistor R_t is the same as the one charging the capacitor C_t. It has to be considered that the resistor R_t which can be any arbitrary resistive component, e. g. NTC-resistor, PTC-resistor, magneto resistor or optovoltaic cell, does not fall below a value of $R_t = 1\ k\Omega$. That means a positive voltage of $V_t = 2.5$ V is allowed as a minimum value for operation with a constant-voltage source. Below these limits the output of FZK 101 has the state Q = H. Operation of the FZK 101, however, is admissible to values of $V_t = 0$ V and $R_t = 0\ \Omega$. Only negative values of V_t destroy the FZH 101. The upper limit of the capacitance is determined by the amount of the capacitor leakage current. Electrolytic capacitors with a capacitance of 100 µF may have leakage currents in the order of the charging currents of this circuit. Therefore the correct function is only guaranteed at values of $C_t < 100\ \mu F$.

The series resistors with a value of 100 Ω each decrease the influence of temperature variations.

List of parts:

1 FZH 101, Q 67000-K 6
2 BC 178 B, Q 62702-C 154

9. Analog circuits

9.1 Light barriers using TAA 761 A, TCA 105, TCA 325 A and TCA 345 A

In the following some light barrier circuits are described. The LED LD 261 is the light emitting component in all cases. The optimal current of this diode is about 10 mA and it is adjusted by the series resistor R_1. In accordance to the used operating voltage R_1 is obtained as follows:

V_S	3	5	9	12	15	18	24 V
R_1	0.1	0.33	0.68	1.0	1.3	1.6	2.2 kΩ

A distance of 10 mm between emitter and receiver is achievable. Greater distances require additional optics, whereby an adjusting device for emitter or receiver has to be taken into consideration. The outputs in the circuits described are defined as follows:

BPX 81 illuminated: output Q = L-signal (conducting)
output $\overline{Q}$ = H-signal (non-conducting)

Fig. 9.1 a shows a light barrier circuit which is suitable for the op amps TAA 761 A and TCA 325 A. Both op amps differ essentially by their output stages. TAA 761 A has a Darlington circuit and includes a terminal for frequency compensation (pin 6). Since applications of switching amplifiers generally do not require any frequency compensation, pin 6 of TAA 761 A is not connected. The TAA 761 A is used advantageously with applications where the output voltage is negligible in the conducting state, e. g. with operations of LSL-circuits, relays etc.

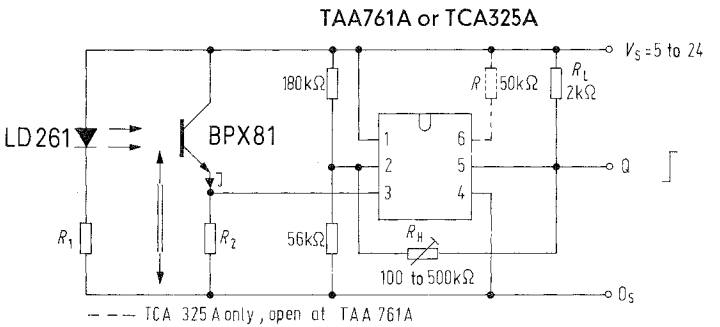


Fig. 9.1 a

However fort those applications requiring low output voltages, e. g. for driving TTL-circuits, the op amp TCA 325 A has to be used, since it has only a simple output transistor. The collector of the driving stage is connected to pin 6 and an additional resistor R is required. As this collector current has to be min. 4 % of the output current I_Q, the resistance R is roughly calculated by the relationship $R = 25 \times R_L$.

The threshold of the op amp is determined by the voltage divider at the non-inverting input (pin 2) and the hysteresis is adjusted by the coupling resistor R_H. For a rough estimation it can be assumed that R_H is in parallel to the resistor of 56 kΩ if the photo transistor is illuminated and in series to the resistor of 180 kΩ in the dark stage. In this case optimum values for R_H are between 100 kΩ and 500 kΩ. By that a resulting hysteresis voltage having a value between 30 % and 10 % of the supply voltage V_S is applied at pin 2.

The operating current I of the photo transistor has to be adjusted by the resistor R_2 in accordance with the chosen operating voltage, the illuminance and the sensitivity group of the BPX 81. As the quantity of light supplied to the photo transistor depends on distance, position, other light sources superimposed and the radiant power group of the LD 261 a trial run is recommended to obtain optimum adjustment. In case of other external light source influences a safe operation is achieved at $I \sim 100\ \mu A$.

The circuit is suitable for all groups of the components LD 261 and BPX 81.

In **Fig. 9.1 b** a very simple circuit of a light barrier using the integrated threshold switch TCA 105 is shown. At pin 2 the base of the input transistor of the TCA 105 is accessible and at pin 3 the emitter. The base is connected internally with the collector via a resistor of about 8 kΩ. The direction of the resulting current determines now the output state of the TCA 105. Is the current allowed to flow via the input pin 2 then the output transistor of pin 5 is non-conductive and the one of pin 4 is conductive. This refers to the illuminated state of the photo transistor BPX 81. The switching current required at pin 2 amounts about 80 μA. The current flow is interrupted by covering the BPX 81.

By its base current flowing now the input transistor is switched on. The output at pin 5 is conductive and the one at pin 4 is inhibited.

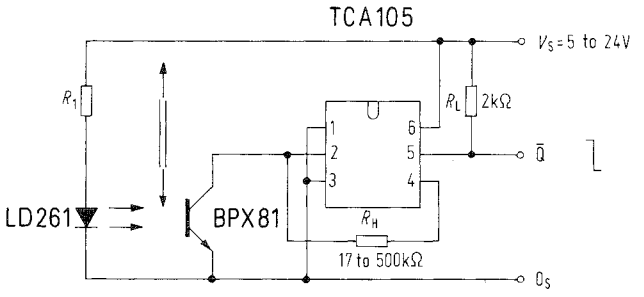


Fig. 9.1 b

The switching hysteresis of the TCA 105 is increased by the resistor R_{II}. During the illuminated state the output 4 is conductive. Thus a part of the input current at pin 2 flows via R_{II} and the output transistor. Resistances of less than 15 kΩ have to be avoided for R_{II}, otherwise self-interlocking may occur. If the circuit is operated in this way additional measures at output pin 4 are not possible. By the resistor R_{II} the cut-off threshold is reduced by the following factor referred to the switch-on threshold:

R_{II}:	17	20	50	100	250	500 kΩ
Reduction factor:	30	25	10	5	2	1 %

With this circuit it is impossible to adjust the photo current of the BPX 81. Therefore only photo transistors of sensitivity group III and VI are suited. If required the sensitivity of the circuit may be changed by variation of the LED-current.

A relatively higher sensitivity as well as a better hysteresis is offered by the circuit shown in **Fig. 9.1 c.** An additional transistor BCW 60 is used. Now the hysteresis is adjusted by resistor R_{II} between pin 5 and the base resistor of 10 kΩ. For a rough calculation it may assumed that R_{II} is in parallel to the base resistor.

If the photo transistor is illuminated the output at pin 5 is turned off and R_H is connected to the supply voltage via the collector resistor. Therefore the cut-off threshold is reduced by the base current flowing additionally via R_H. The hysteresis is determined by the supply voltage and the resistor R_H. In the following table the resistances required are indicated. A hysteresis variation of about 20 % to 50 % referred to the starting current is obtained by the potentiometer P.

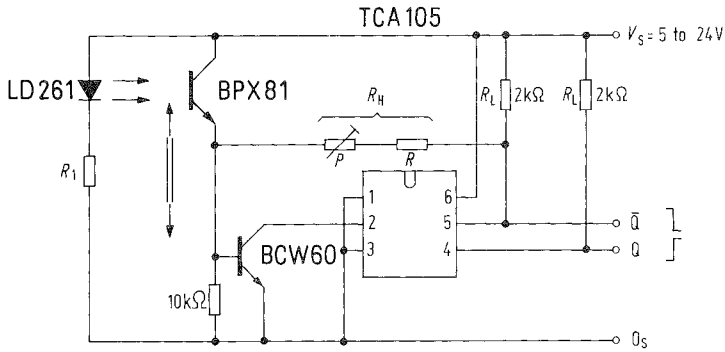


Fig. 9.1 c

V_S = 5 V:	R = 150 kΩ	P = 100 kΩ
V_S = 10 V:	R = 270 kΩ	P = 250 kΩ
V_S = 15 V:	R = 390 kΩ	P = 250 kΩ
V_S = 20 V:	R = 560 kΩ	P = 250 kΩ
V_S = 24 V:	R = 680 kΩ	P = 500 kΩ

The lower limit of the resistance R_H is determined by the operating voltage V_S and it is for instance R_H = 100 kΩ at V_S = 5 V. For lower values a self-interlocking occurs. An adjustment of the photo current is possible by variation of the base resistance, but in this case the resistance R_H has also to be changed accordingly. Since the permissible output current is 50 mA also small relays can be driven directly.
Threshold and hysteresis of the integrated threshold switch TCA 345 A are determined by the operating voltage V_S. An approximate value for the hysteresis at input pin 1 is $V_H \sim 0.25\ V_S$.

The permissible output current is 70 mA and therefore small relays can be connected directly. A protection of the output transistor is not necessary, since all diodes required are incorporated into the TCA 345 A. A suitable circuit with a light barrier is shown in **Fig. 9.1 d.** The photo current I of the BPX 81 has to be adjusted by the resistor R_2 in accordance to the operating voltage, the illuminance and the sensitivity group of the photo transistor. Since the quantity of light applied to the BPX 81 depends on distance, position, other light sources and the radiant power group of the LD 261 a trial run is recommended to attain optimal adjustment. In case of other external light source influences a safe operation is achieved at $I \sim 100\ \mu A$. Thus the following guideline values have been experienced for the resistor R_2:

V_S	3	5	7 V
R_2	15	22	33 kΩ

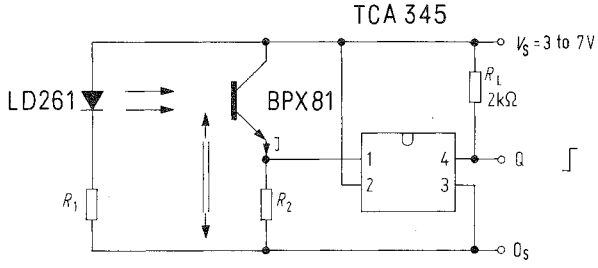


Fig. 9.1 d

List of parts:

1 TCA 761 A or TAA 761, Q 67000-A 522 or Q 67000-A 224
1 TCA 105, Q 67000-A 527
1 TCA 325 A, Q 67000-A 562
1 TCA 345 A, Q 67000-A 564
1 BPX 81, Q 62702-P 20
1 BCW 60, Q 62702-C 331 to C 333
1 LD 261, Q 62703-Q 63.

9.2 Lux-meter using TCA 335 A

In **Fig. 9.2** a circuit of a simple lux-meter is shown, where the op amp TCA 335 A and a silicon photo diode BPX 91 are used.

by the optical filter BG 38; 2 mm, produced by Messrs. Schott-Mainz, the spectral sensitivity of the photo diode corresponds to that of the human eye.
The sensitivity range is chosen decadicly between 10^2 to 10^5 lux by the switch S. A moving-coil instrument with a full-scale deflection of 100 µA operates as an indicator.

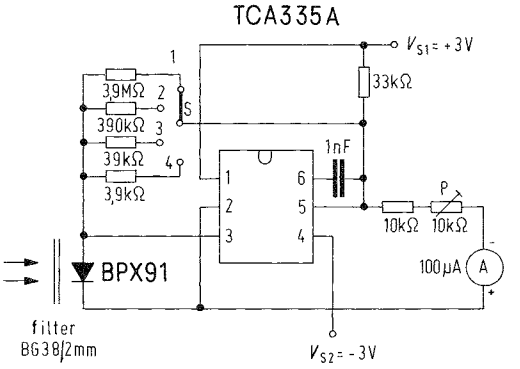


Fig. 9.2

The photo diode is connected between the inverting and non-inverting input (pin 2 and 3) of the TCA 335 A. Therefore the BPX 91 runs in short-circuit operation up to lowest illuminances and a good linearity of this circuit is achieved. The error in measurement is determined by the required input current of the op amp TCA 335 A and the following relation is valid:

$$\text{Error } F = \frac{I_i}{E_V \times S} \times D$$

whereat:

I_i = input current of the TCA 335 A in nA
E_V = illuminance in lux
S = sensitivity of the BPX 91 in $\frac{\text{nA}}{\text{lux}}$
D = attenuation factor of the filter BG 38

Under the condition of $E_V = 100$ lx and the consideration of the respective cut-off frequency the error in measurement amounts to:

$$F = \frac{50}{100 \times 35} \times 8 \sim 0.1 = 10\ \%$$

For typical values the error F is about 3 %.

The full-scale of the instrument is adjusted by the potentiometer P. Instruments with a full-scale of 1 mA may be used, too. In this case the value of the series resistor has to be decreased. The accuracy of indication is determined by the tolerance of the precision resistors 39 kΩ, 390 kΩ and 3.9 kΩ.

A gain decrease at higher frequencies is achieved by a capacitor of 1 nF at pin 6. By that a tendency towards oscillation is safely avoided. This luxmeter may be powered by two batteries, since the measurement accuracy is independent of supply voltage variations.

Technical data:

Supply voltage	V_S	$\pm$ 3 V
Supply current	I_S	0.5 mA
Measurement ranges at full-scale	E_V	10^2 to 10^5 lx
Temperature coefficient	α	$+ 0.2 \frac{\%}{K}$
Max. output current	I	< 1 mA

List of parts:

1 TCA 335 A, Q 67000-A 563
1 BPX 91, Q62702-P 48

9.3 Proximity detector using TCA 105

In the following section three different applications for an inductive proximity detector with the integrated threshold switch TCA 105 are described. The two anti-valent outputs are defined always as follows:
Oscillator operates:

output Q = L-state (conductive)
output Q = H-state (non-conductive)

If the oscillation is interrupted the outputs have the complementary state.

Figure 9.3 a shows a very economical solution for an inductively operating proximity detector, where a piece of metal is used to complete the magnetic circuit. The input transistor of the TCA 105 and the two inductances 1.25 and 4.5 μH operate as a Hartley oscillator. Pulse shape and frequency are determined mainly by dimensioning of the coils. With suitable cores, e.g. Siferrit-pot cores B 65511-M 000-R 025 or B 65531-K 0040-A 001 and inductances mentioned

above an oscillation is achieved at typical frequencies between 2 and 3 MHz and between 1 and 10 MHz if the coil data are varied.
Operations at frequencies below 1 MHz are critical ones, since the oscillation may be superposed on the output state.

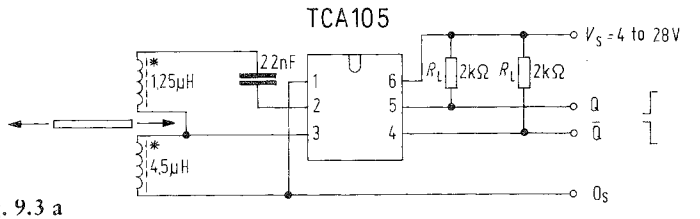


Fig. 9.3 a

The oscillation is interrupted as soon as a piece of iron is inserted between the two coils. The permissible slot width is about 5 mm, if the electrical circuit is optimal proportioned. Seperation of the different potentials is achieved by the blocking capacitor of 22 nF.
In **Fig. 9.3 b** a similar circuit for a detector is shown. In this case the coils are influenced by a piece of metal moved infront of the inductances. The oscillator circuit consists of $L_1 = 12.5$ µH and $C = 470$ pF determining mainly the frequency. The oscillation is interrupted, if a piece of metal attenuates the resonant circuit. The metal may be approximated in horizontal as well as in vertical direction. Starting of oscillation is adjustable by the potentiometer $P = 1$ kΩ controlling the attenuation of the circuit. By that it is possible to set threshold in the way, that a piece of metal achieves a switching of the TCA 105 at an approximation in horizontal direction to a minimum distance of 1 mm.

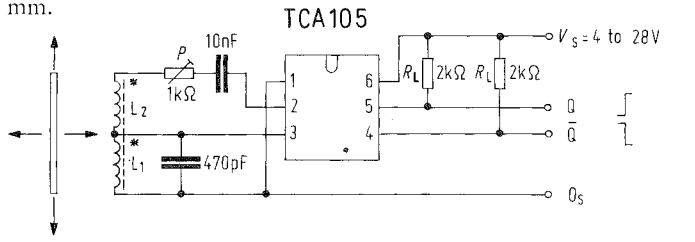


Fig. 9.3 b

The switching hysteresis is 0.2 mm on the average. If the piece of metal is moved in vertical direction the hysteresis as well as the threshold are determined in addition by the horizontal distance to the core.

The switching characteristics are inversely proportional to the distance, that means safer switching at smaller distances. But optimal results will be obtained only by a practical trial run. The following guideline data have been experienced: hysteresis of 0.6 to 0.7 mm at distances of 0.5 mm.

Siferrit-pot cores, e.g. type B 65517-A 0000-R 001 are suitable components for the oscillator. If a wire of 0.1 mm CuL is used the turns required for one half of a core with the demensions of 9 × 5 mm are as follows:

L_1: n_1 = 20 turns,
L_2: n_2 = 7 turns.

For proximity switches showing a higher sensitivity an additional transistor stage is required (see **Fig. 9.3 c**). Adjustment potentiometers for hysteresis (P_1) and sensitivity in accordance to the distance (P_2) enable the construction of a very accurate proximity switch operating between distances of 0.3 and 10 mm and offering a hysteresis of 0.3 to 1 mm according to the chosen distance. An attenuation is possible by approximation in vertical as well as in horizontal direction.

List of parts:
1 TCA 105, Q 67000-A 527
1 BC 237, Q 62702-C 276 and C 277

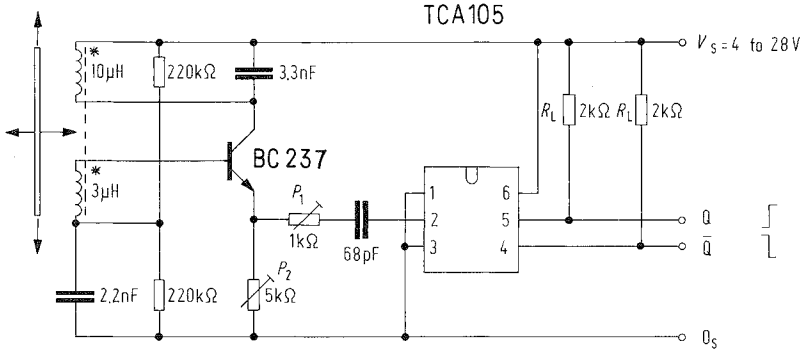


Fig. 9.3 c

9.4 Threshold switch using TCA 105

Fig. 9.4 shows a very simple threshold switch, current controlled. It is proportioned in the way that the input transistor of the TCA 105 is switched off during the quiescent state $I_1 = 0$. By that the output Q (pin 5) is conductive and the output $\bar{Q}$ (pin 4) non-conductive. As

soon as an additional current is applied to the input I, its first transistor is turned on. Then the outputs switch to the complementary state.

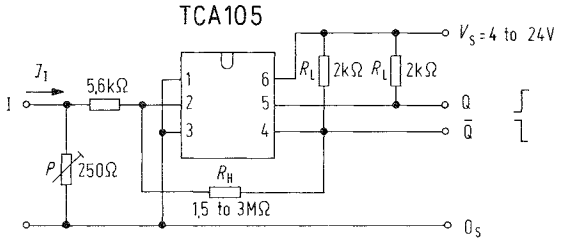


Fig. 9.4

The circuit flips as soon as the input current generates a voltage drop of about 200 mV at the resistor P = 250 Ω. The tolerance expected for different TCA 105 is approximately ± 50 mV. Therefore the required input sensitivity can be adjusted by the potentiometer P. The circuit shown in Fig. 9.4 is proportioned for a threshold of I_I = 2 mA. Other currents are attained by suitable matching of the input impedance.

The switching hysteresis is adjusted by the resistor R_H with a wide-range resistance variation. The resulting hysteresis amounts approximately I_{HI} = 100 to 400 µA at the resistance range indicated. Furthermore it has to be considered that also the value of the load resistor R_L at pin 4 as well as the chosen supply voltage V_S determine the hysteresis. Favourable values are as follows: R_L less than 60 kΩ and R_H more than 1 MΩ.

List of parts:

1 TCA 105, Q 67000-A 527

10. AM-receiver with TCA 440

The AM-receiver circuit TCA 440 consists of two control systems which operate independently of each other and which act on the pre-stage as well as upon the IF-stages (refer to **Fig. 10 a**). Due to the pre-stage control an excellent large signal stability is achieved. A voltage of 2.6 V_{pp} at the TCA 440 input is processed with low distortions only. The balanced mixer operates multiplicative. Therefore only a few harmonic mixing products and squealings are generated. It is impossible to influence the oscillator, seperated from the mixer, by any signal at the input. From the control circuit of the IF-amplifier an adjustment indication voltage is obtained, thus a moving-coil instrument can be connected directly and the following data are recommended: 500 µA (R_i = 800 Ω) or 300 µA (R_i = 1.5 kΩ). The symmetrical construction of the total integrated circuit achieves not only a high stability against unwanted oscillations but also a control range of more than 100 db. The bridge circuit of the mixer suppresses a direct IF-interference. Thereby the formerly feared tendency towards oscillations at the lower end of the MF-band is eliminated.

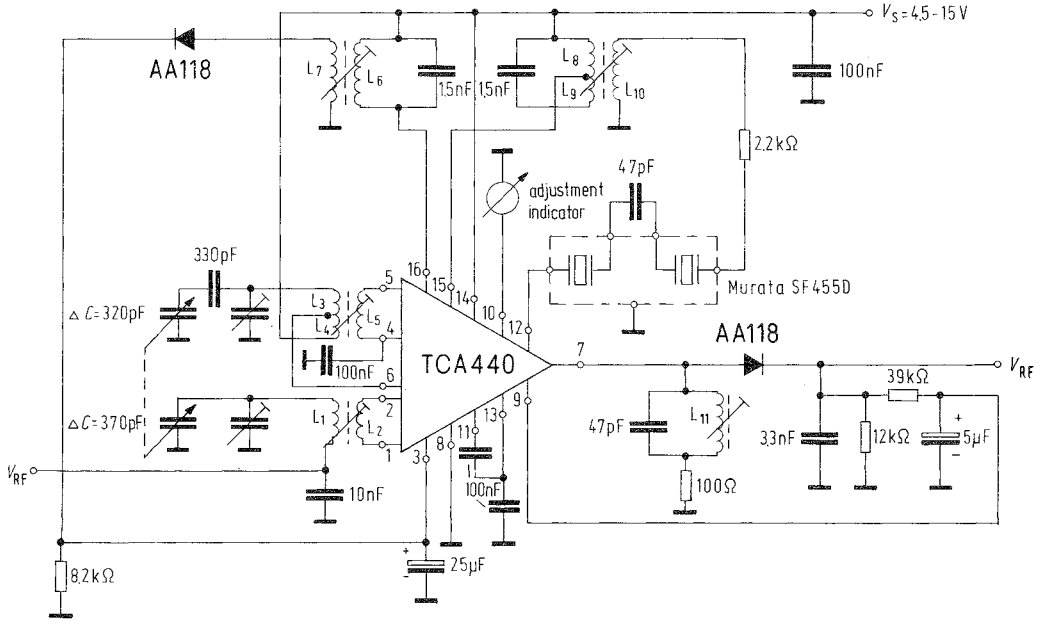


Fig. 10 a

With applications of tuning diodes BB 113 (**Fig. 10 b**) a seperated prestage control is no longer convenient, since with voltages of more than 1 V_{eff} at the input circuit there are already distortions. In the best way the voltage for the prestage control is derived from the IF-control voltage. In this case the pins 3 and 10 have to be connected directly. The LC-circuit at pin 16 is no longer necessary. Now the stability against large signals is lowered by 5 db. At a diode voltage of $V_D = 6$ V the input frequency amounts $f_{RF} = 850$ kHz and at $V_D = 30$ V it is $f_{RF} = 1650$ kHz.

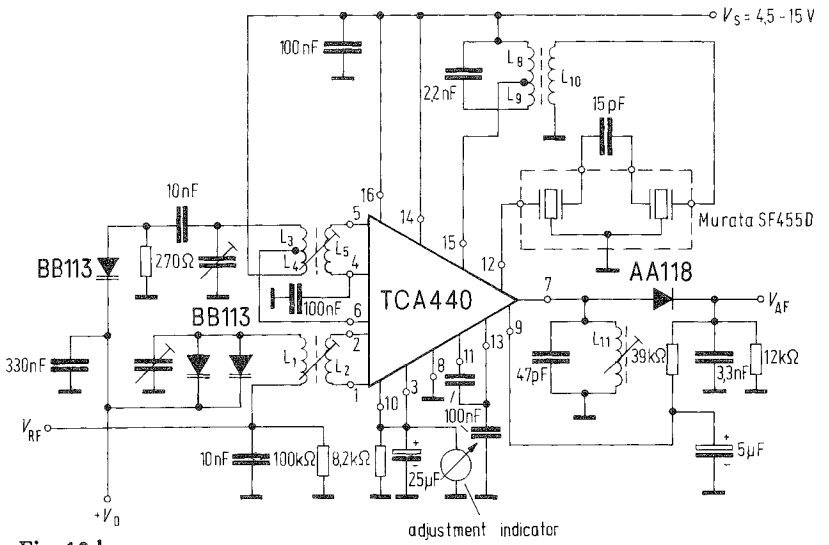


Fig. 10 b

Technical data:

Operating voltage	V_S	4.5 to 15 V
Current consumption at $V_S = 9$ V	I_S	10.5 mA
Input sensitivity		
($V_S = 9$ V, $f_i = 1$ MHz, m = 30 % and 0 %)		
at a signal-to-noise ratio of 26 db	V_{RF}	7 µV
AF-output voltage for V_{RF}		
symmetrically measured at 1–2		
(m = 30 %; $V_S = 9$ V)		
$V_{RF} = 20$ µV	$V_{AF\,eff}$	50 mV
$V_{RF} = 500$ mV	$V_{AF\,eff}$	130 mV

Winding data for the coils

$L_1 : n_1 = 105$ turns 12×0.04 CuLS
$L_2 : n_2 = 7$ turns 0.10 CuL
$L_3 : n_3 = 80$ turns 12×0.04 CuLS
$L_4 : n_4 = 35$ turns 12×0.04 CuLS
$L_5 : n_5 = 15$ turns 0.10 CuL
$L_6 : n_6 = 70$ turns 12×0.04 CuLS
$L_7 : n_7 = 35$ turns 12×0.04 CuLS
$L_8 : n_8 = 20$ turns 12×0.04 CuLS
$L_9 : n_9 = 50$ turns 12×0.04 CuLS
$L_{10} : n_{10} = 22$ turns 12×0.04 CuLS
$L_{11} : n_{11} = 400$ turns 0.06 CuL
L_1–L_2 mounted on Voigt-kit D 21-2375.1
L_3–L_{11} mounted on Voigt-kit D 41-2519

List of parts:

1 TCA 440, Q 67000-A 669
3 BB 113, Q 62702-B 41
1 AA 118, Q 60101-X 118